



# Systems Quality/Reliability Handbook



Order Number: 231762-002



# LITERATURE

To order Intel literature write or call:

Intel Literature Sales  
P.O. Box 58130  
Santa Clara, CA 95052-8130

Toll Free Number:  
(800) 548-4725\*

Use the order blank on the facing page or call our Toll Free Number listed above to order literature. Remember to add your local sales tax and a 10% postage charge for U.S. and Canada customers, 20% for customers outside the U.S. Prices are subject to change.

## 1988 HANDBOOKS

Product line handbooks contain data sheets, application notes, article reprints and other design information.

NAME	ORDER NUMBER	**PRICE IN U.S. DOLLARS
<b>COMPLETE SET OF 8 HANDBOOKS</b> Save \$50.00 off the retail price of \$175.00	231003	\$125.00
<b>AUTOMOTIVE HANDBOOK</b> (Not included in handbook Set)	231792	\$20.00
<b>COMPONENTS QUALITY/RELIABILITY HANDBOOK</b> (Available in July)	210997	\$20.00
<b>EMBEDDED CONTROLLER HANDBOOK</b> (2 Volume Set)	210918	\$23.00
<b>MEMORY COMPONENTS HANDBOOK</b>	210830	\$18.00
<b>MICROCOMMUNICATIONS HANDBOOK</b>	231658	\$22.00
<b>MICROPROCESSOR AND PERIPHERAL HANDBOOK</b> (2 Volume Set)	230843	\$25.00
<b>MILITARY HANDBOOK</b> (Not included in handbook Set)	210461	\$18.00
<b>OEM BOARDS AND SYSTEMS HANDBOOK</b>	280407	\$18.00
<b>PROGRAMMABLE LOGIC HANDBOOK</b>	296083	\$18.00
<b>SYSTEMS QUALITY/RELIABILITY HANDBOOK</b>	231762	\$20.00
<b>PRODUCT GUIDE</b> Overview of Intel's complete product lines	210846	N/C
<b>DEVELOPMENT TOOLS CATALOG</b>	280199	N/C
<b>INTEL PACKAGING OUTLINES AND DIMENSIONS</b> Packaging types, number of leads, etc.	231369	N/C
<b>LITERATURE PRICE LIST</b> List of Intel Literature	210620	N/C

\*Good in the U.S. and Canada

\*\*These prices are for the U.S. and Canada only. In Europe and other international locations, please contact your local Intel Sales Office or Distributor for literature prices.

*About Our Cover:*

*The quality and reliability of a great system is based on a blending of building blocks—some repetitive, some unique, but all impeccable. Together these elements can couple elegant design with robust purpose. The result merges timeless art into dependable function.*





*Intel the Microcomputer Company:*

*When Intel invented the microprocessor in 1971, it created the era of microcomputers. Whether used as microcontrollers in automobiles or microwave ovens, or as personal computers or supercomputers, Intel's microcomputers have always offered leading-edge technology. In the second half of the 1980s, Intel architectures have held at least a 75% market share of microprocessors at 16 bits and above. Intel continues to strive for the highest standards in memory, microcomputer components, modules, and systems to give its customers the best possible competitive advantages.*

## **SYSTEMS QUALITY/RELIABILITY HANDBOOK**

**1988**





Intel Corporation makes no warranty for the use of its products and assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

Intel retains the right to make changes to these specifications at any time, without notice.

Contact your local sales office to obtain the latest specifications before placing your order.

The following are trademarks of Intel Corporation and may only be used to identify Intel Products:

Above, BITBUS, COMMputer, CREDIT, Data Pipeline, FASTPATH, GENIUS, i, i<sup>2</sup>, ICE, iCEL, iCS, iDBP, iDIS, i<sup>2</sup>ICE, iLBX, i<sub>m</sub>, iMDDX, iMMX, Inboard, Insite, Intel, int<sub>el</sub>, int<sub>el</sub>BOS, Intel Certified, Intelelevision, int<sub>el</sub>igent Identifier, int<sub>el</sub>igent Programming, Intellec, Intellink, iOSP, iPDS, iPSC, iRMK, iRMX, iSBC, iSBX, iSDM, iSXM, KEPROM, Library Manager, MAP-NET, MCS, Megachassis, MICROMAINFRAME, MULTIBUS, MULTICHANNEL, MULTIMODULE, MultiSERVER, ONCE, OpenNET, OTP, PC-BUBBLE, Plug-A-Bubble, PROMPT, Promware, QUEST, QueX, Quick-Pulse Programming, Ripplemode, RMX/80, RUPI, Seamless, SLD, SugarCube, SupportNET, UPI, and VLSiCEL, and the combination of ICE, iCS, iRMX, iSBC, iSBX, iSXM, MCS, or UPI and a numerical suffix, 4-SITE.

MDS is an ordering code only and is not used as a product name or trademark. MDS® is a registered trademark of Mohawk Data Sciences Corporation.

\*MULTIBUS is a patented Intel bus.

Additional copies of this manual or other Intel literature may be obtained from:

Intel Corporation  
Literature Distribution  
Mail Stop SC6-59  
3065 Bowers Avenue  
Santa Clara, CA 95051



# TABLE OF CONTENTS

## OVERVIEW

Systems Quality/Reliability Overview .....	I
--	---

## CHAPTER 1

### Materials Quality

Corporate Materials Quality Charter .....	1-1
Site Materials Quality Charter .....	1-2
Dock-to-Stock .....	1-5
Just-in-Time Manufacturing .....	1-5
Commodity Management .....	1-5
Statistical Process Control Program .....	1-8
Part Qualification .....	1-11
Supplier Qualification .....	1-12
Ongoing Maintenance of Parts and Supplier Quality .....	1-12
Purchased Product Programs .....	1-13
Materials Quality Inspection .....	1-16
Materials Flow Control .....	1-18

## CHAPTER 2

### Reliability

Reliability Program .....	2-1
Reliability Specification .....	2-1
Reliability Plan .....	2-2
MTBF Prediction .....	2-2
Reliability Bathtub Curve Review .....	2-3
Reliability Testing .....	2-5
Reliability Report .....	2-9
MTBF Versus Operating Temperature and Duty Cycle .....	2-12
Audit Kit .....	2-14
Field Reliability .....	2-14
Reliability Database .....	2-15
Reliability Qualification of New Technology .....	2-15
Environmental Specification .....	2-16
Environmental/Reliability Laboratory .....	2-17

## CHAPTER 3

### Manufacturing

A Commitment to World-Class Manufacturing .....	3-1
Product Lines and Technology .....	3-1
Manufacturing Capability .....	3-4
Key Strategies for Manufacturing Quality and Reliability .....	3-5
Board Manufacturing .....	3-7
Systems Manufacturing .....	3-16
Software Manufacturing .....	3-19



Control Systems .....	3-20
Manufacturing SPC Program .....	3-22
Production Facility Evaluation Program .....	3-25
Human Resource Development .....	3-28

## **CHAPTER 4**

### **Product Regulations**

Reliance on External Standards .....	4-1
Product Safety Council .....	4-1
Prevention .....	4-2
Certification .....	4-5
Traceability .....	4-7
Safety Training .....	4-8

## **CHAPTER 5**

### **Field Activities**

Customer Quality Engineering .....	5-1
Customer Support Centers .....	5-1
Indicator Reports .....	5-1
Warehouse Audits .....	5-3
Applications Support .....	5-4
Field Quality Improvement Teams .....	5-4
Field Relations .....	5-5

## **CHAPTER 6**

### **Support**

Corporate Components Engineering .....	6-1
Peripherals and Power Supply Engineering .....	6-7
Systems Document Control Center .....	6-12
Worldwide Support .....	6-15
Contract Review .....	6-25

## **APPENDIX**

STATISTICAL PROCESS CONTROL TOOLS .....	A-1
---	-----

<b>GLOSSARY</b> .....	G-1
-----------------------	-----



## PREFACE

### THE CHIEF EXECUTIVE OFFICER'S VIEW OF QUALITY

Product quality and reliability are fundamental requirements for success in today's high-tech marketplace. Never before have customers demanded such high levels of perfection. We, by driving quality and reliability to levels labeled impossible just a few years ago, hope to continually exceed our customers' expectations.

No activity requires greater commitment to quality and reliability than the manufacturing of VLSI (Very Large Scale Integration) components and VLSI-based computer systems. In such components and systems, millions of integrated transistors must operate for long periods without error or failure. To this end, the Intel Systems Group supplies many of the world's most advanced VLSI-based computer products.

Although some people think of Intel as a semiconductor company, the truth is that we've been producing and selling system-level products almost since our inception—1970 to be exact. Today, we develop, manufacture and support dozens of different building blocks for microcomputer systems. These include board- and systems-level products that support three industry-standard bus architectures (MULTIBUS® I, MULTIBUS® II, and AT Bus); networking products; and development tools for Intel architectures on a variety of hosts.

This handbook describes Intel's approach and procedures for maintaining our system product quality and reliability. We hope this book provides you with useful insights into our programs. Intel is committed to being a leading supplier of the highest-quality, highest-reliability systems products.

*Andy Grove*

A.S. Grove  
President and Chief Executive Officer



---

## **CUSTOMER SUPPORT**

### **CUSTOMER SUPPORT**

Customer Support is Intel's complete support service that provides Intel customers with hardware support, software support, customer training, and consulting services. For more information contact your local sales offices.

After a customer purchases any system hardware or software product, service and support become major factors in determining whether that product will continue to meet a customer's expectations. Such support requires an international support organization and a breadth of programs to meet a variety of customer needs. As you might expect, Intel's customer support is quite extensive. It includes factory repair services and worldwide field service offices providing hardware repair services, software support services, customer training classes, and consulting services.

### **HARDWARE SUPPORT SERVICES**

Intel is committed to providing an international service support package through a wide variety of service offerings available from Intel Hardware Support.

### **SOFTWARE SUPPORT SERVICES**

Intel's software support consists of two levels of contracts. Standard support includes TIPS (Technical Information Phone Service), updates and subscription service (product-specific troubleshooting guides and COMMENTS Magazine). Basic support includes updates and the subscription service. Contracts are sold in environments which represent product groupings (i.e., iRMX environment).

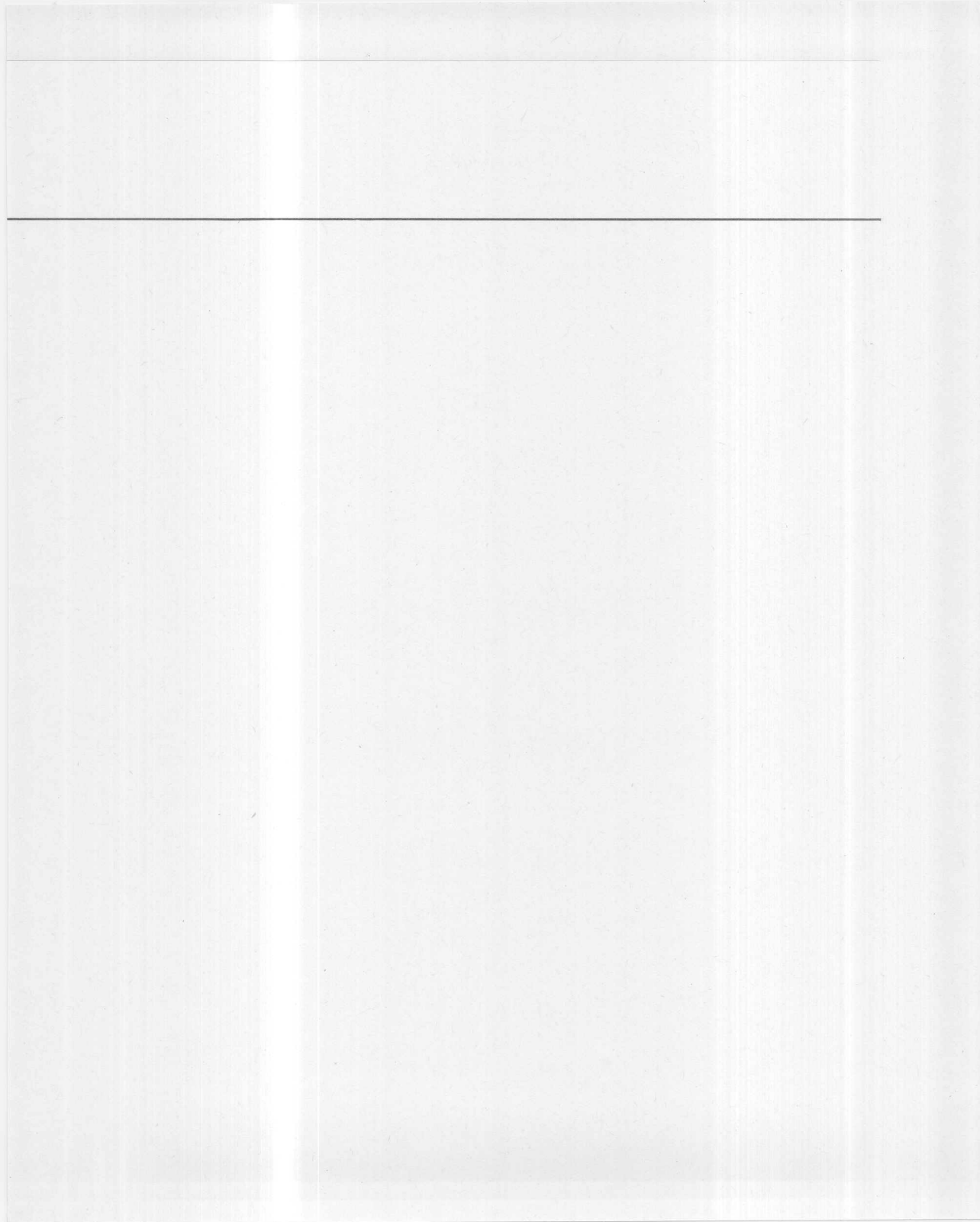
### **CONSULTING SERVICES**

Intel provides field systems engineering services for any phase of your development or support effort. You can use our systems engineers in a variety of ways ranging from assistance in using a new product, developing an application, personalizing training, and customizing or tailoring an Intel product to providing technical and management consulting. Systems Engineers are well versed in technical areas such as microcommunications, real-time applications, embedded microcontrollers, and network services. You know your application needs; we know our products. Working together we can help you get a successful product to market in the least possible time.

### **CUSTOMER TRAINING**

Intel offers a wide range of instructional programs covering various aspects of system design and implementation. In just three to ten days a limited number of individuals learn more in a single workshop than in weeks of self-study. For optimum convenience, workshops are scheduled regularly at Training Centers worldwide or we can take our workshops to you for on-site instruction. Covering a wide variety of topics, Intel's major course categories include: architecture and assembly language, programming and operating systems, bitbus and LAN applications.







## **OVERVIEW**

### **SYSTEM QUALITY/RELIABILITY**

#### **INTRODUCTION**

One of Intel's corporate objectives is to be and be recognized as the leader in meeting customers' needs for delivery, quality, reliability and service. Since its inception in 1978, the Systems Group has done just that. We have met or exceeded our customers' expectations for quality and reliability for all products introduced.

Intel's world-class stature in the area of quality and reliability is the result of four management tenets:

First, it is Intel's management philosophy that quality and reliability are everyone's charters. Quality and reliability goals are considered integral parts of every business operation and are established and evaluated annually in Strategic Long Range Plans. Individuals, as well as business operations, include quality and reliability goals as part of their quarterly objectives and key results.

Second, any new Intel systems product or upgrade must pass extensive quality and reliability guidelines before being released in the marketplace. Quality and reliability standards are set at the initial proposal of a new technology or new product development cycle. We've developed an entire quality and reliability curriculum to assure design engineers, auditors, manufacturing personnel and managers understand and can implement Intel's quality standards.

Third, Intel devotes considerable research and development resources to advancing reliability and environmental testing, quality engineering and failure analysis capabilities.

Fourth, we're continually sounding our markets and competitors to assure that we can hold a dominant position in our chosen market areas.

#### **FACILITIES**

Intel Systems Group facilities include design, manufacturing, sales, marketing and customer service centers located in Europe, Israel, Japan, Hong Kong, Singapore and North America. (Manufacturing plants are located in Puerto Rico, Singapore, and the U.S.) We have major customer service centers in England, Japan and the U.S. and are able to link these sites through common workmanship standards and manufacturing guidelines. A number of policies and procedures, together with our auditing and monitor programs, guarantee Intel customers consistent products from all manufacturing sites and repair centers.

#### **ORGANIZATION**

Definition and supervision of the Systems Division quality and reliability program is the responsibility of the Systems Quality and Reliability (SQR) organization. SQR reports directly to the vice president of the Systems Group and is heavily matrixed to other organizations in the

Systems Group, such as engineering, manufacturing, marketing, sales and customer service. Figure 1-1 shows the relationship of the SQR group to the rest of the Systems Group; Figure 1-2 shows the inter-divisional matrixing of SQR with other Systems Group groups; and Figure 1-3 shows how SQR's responsibilities differ from those of matrixed groups (in this case, manufacturing).

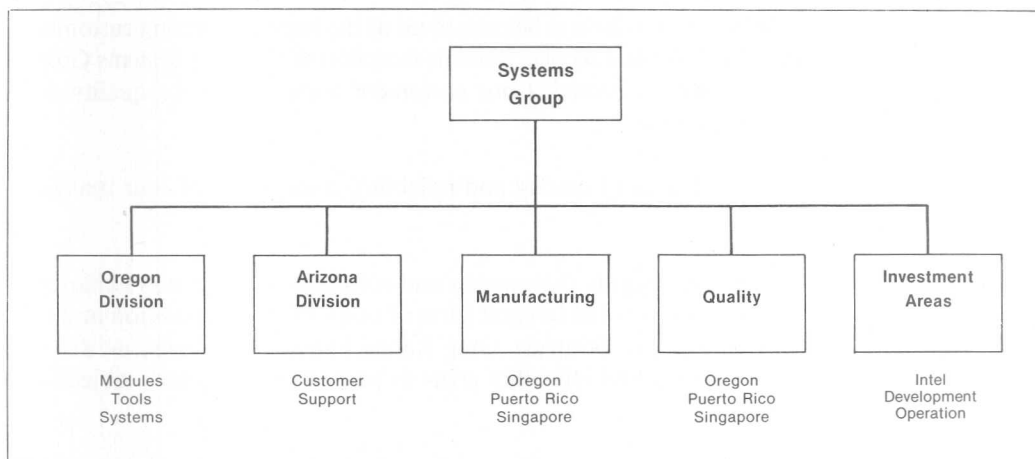


Figure 1. Systems Group Organizational Chart

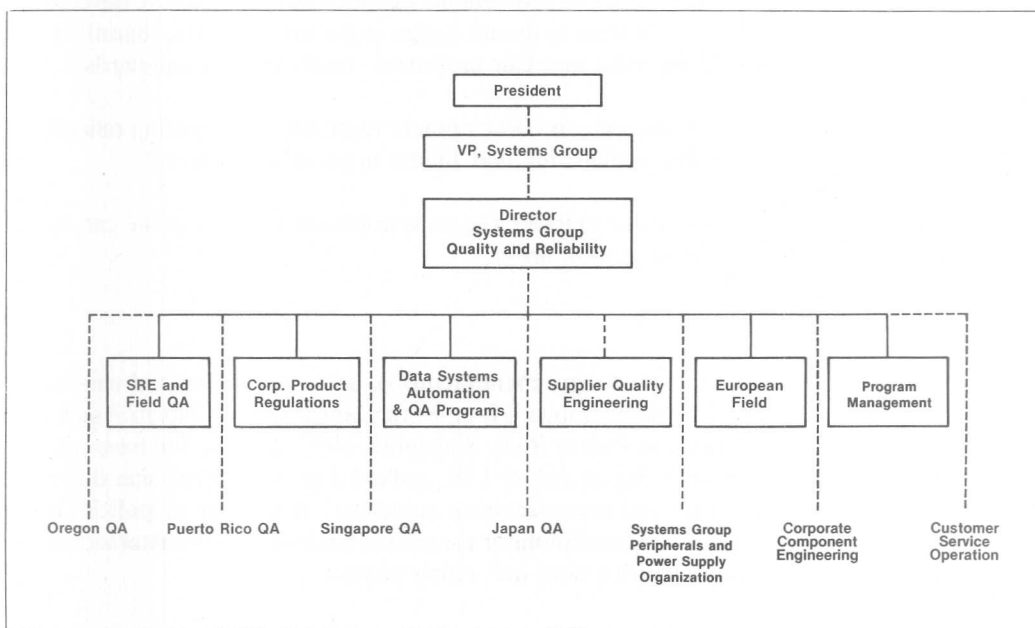


Figure 2. SQR Matrix Diagram



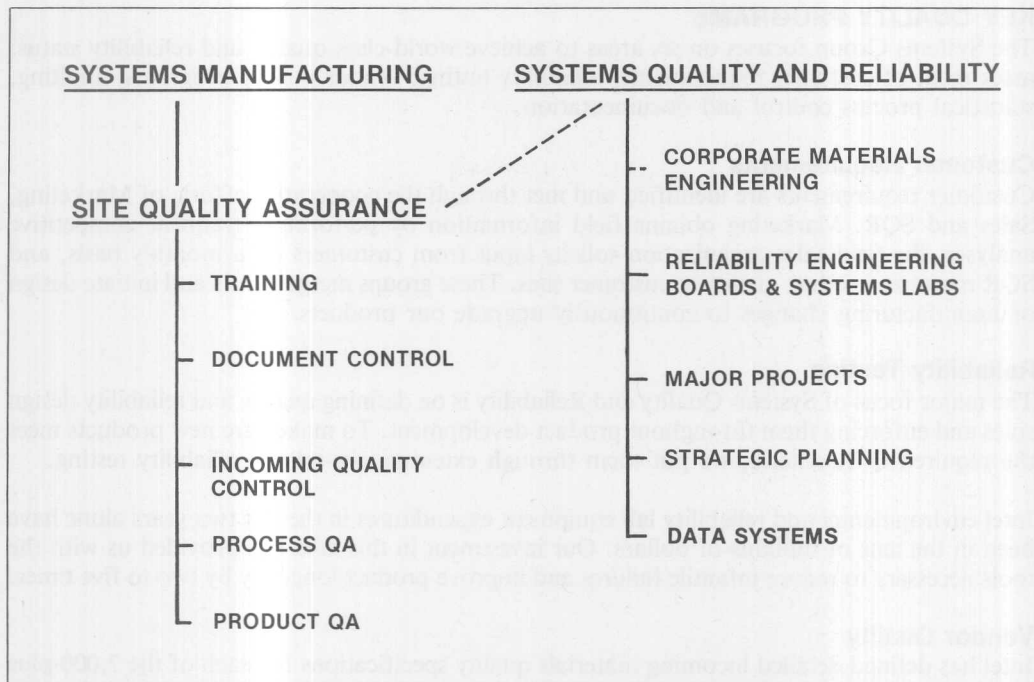


Figure 3. Manufacturing vs. SQR Responsibilities

### PRODUCT DEFINITION

SQR's activities map into Intel's new product development process, which is a five-phase activity:

- Phase 0** This is the product planning stage when product and market requirements are defined, quality and reliability targets set, and overall technical capabilities for meeting those targets defined.
- Phase 1** During Phase 1, we perform in-depth investigation of the marketplace to determine the degree of penetration required, MTBF (mean time between failures) goals, and delivery acceptance/FPA (first pass accept) requirements.
- Phase 2** Phase 2 is the detailed product definition stage during which market feasibility is reviewed to determine customer demands. Product specifications are then drawn up and reviewed. If the product specification meets with approval in the preliminary design review, it is released to design.
- Phase 3** During Phase 3, the design is passed to the product development team, where it undergoes an engineering capability evolution, reliability verification and a test and manufacturability review.
- Phase 4** The final phase of new product development is prototype-build, which determines manufacturing's ability to repeatedly produce the product at the specified quality and reliability goals. At the conclusion of prototype and manufacturing evaluation, the product is transferred to a production facility.

SQR representatives have sign-off authority at every stage, assuring that quality and reliability goals are met through every design or manufacturing phase.

**KEY QUALITY PROGRAMS**

The Systems Group focuses on six areas to achieve world-class quality and reliability status: assessment of customer requirements, reliability testing, vendor quality programs, auditing, statistical process control and documentation.

**Customer Requirements**

Customer requirements are identified and met through the cooperative efforts of Marketing, Sales and SQR. Marketing obtains field information by performing frequent competitive analyses, the field sales organization solicits input from customers on a monthly basis, and SQR monitors product quality at customer sites. These groups merge inputs and initiate design or manufacturing changes to continuously upgrade our products.

**Reliability Testing**

The major focus of Systems Quality and Reliability is on defining quality and reliability design rules and enforcing them throughout product development. To make sure new products meet the required Q/R criteria, we put them through extensive pre-release reliability testing.

Intel environmental and reliability lab equipment expenditures in the last two years alone have been in the tens of millions of dollars. Our investment in this area has provided us with the tools necessary to reduce infantile failures and improve product longevity by two to five times.

**Vendor Quality**

Intel has defined detailed incoming materials quality specifications for each of the 7,000-plus commodities we buy. Our extensive qualification program encompasses characterization, facilities auditing and ongoing parts/product monitoring.

Not only are our own quality standards high, but we insist that suppliers' quality programs be as high as Intel's. We do this by helping suppliers implement or strengthen statistical process control programs throughout their manufacturing process, with the goal of driving full responsibility for materials quality back to the supplier level.

**Auditing**

Intel's audit programs cover many disciplines, from incoming materials to manufacturing. Audits begin at design, move through all five phases of the product development cycle and continue into our factories, repair centers and customer sites.

Audits are tailored to specific processes and performed according to well-defined specifications and procedures.

**Statistical Process Control**

One of the most important factors in Intel's total quality philosophy is the use of statistical process control techniques throughout our factories and facilities.

Statistical Process Control (SPC) is a statistical methodology for identifying, characterizing and reducing the amount of variation in a process. That process can be a manufacturing operation or a sales cycle. By controlling process variation, the production process and the resulting product become more predictable. This leads to the elimination of non-value-added operations such as inspection, test and audit (when we have statistical proof they are no longer needed), with the ultimate benefit being high-quality, cost-competitive products.

The Appendix contains a detailed discussion of SPC tools used at Intel.

**Document Control**

Intel has a central document control center that provides immediate, fully automated document archival and retrieval for all sites. Quality and reliability policies and procedures are constantly updated to reflect current internal and external regulations and serve as up-to-the-minute reference documents for all employees engaged in product design and production.

**CONCLUSION**

Intel Systems Group has established one of the most comprehensive quality/reliability programs in the industry. This handbook presents an overview of these efforts, beginning with incoming materials and extending through customer support.

We feel confident our quality and reliability programs will meet your requirements; in the least, we hope you find our basic strategies and models of execution to be logical and sound.









# CHAPTER 1

## MATERIALS QUALITY

### INTRODUCTION

Intel starts building quality and reliability into its products even before raw materials are received at the loading dock. Our comprehensive supplier quality program is aimed at improving the quality of incoming materials to the point where Intel can move parts from the loading dock to the production line without incoming inspections. Over 50 percent of our systems suppliers are currently at Dock-To-Stock (DTS) inspection levels.

We have statistical process control programs throughout our own and many of our suppliers' factories.

We have detailed supplier and part qualification procedures to ensure that only approved commodities are ordered by Intel manufacturing sites. Our design, manufacturing and inventory data bases are fully integrated to efficiently communicate part approval status/availability information throughout the design-manufacturing-shipping cycle.

Intel's many materials quality programs are managed cooperatively at the corporate and plant levels.

At the corporate level, suppliers, parts and processes are qualified and audited with the goal of moving those suppliers and parts to a dock-to-stock level and ultimately to Just-In-Time (JIT) manufacturing status. At the plant level, parts not approved as DTS are inspected for adherence to Intel's overall and product-specific quality specifications.

### CORPORATE MATERIALS QUALITY CHARTER

Five different organizations within Intel bear the responsibility of supplier/part qualification and quality audits of incoming materials:

**Supplier Quality Engineering (SQE)** is responsible for representing Intel to all suppliers and assuring that incoming materials used in systems manufacturing meet or exceed Intel's quality and reliability specifications. SQE's broad charter is to provide consistency and procedural control for supplier qualification, incoming inspection and ongoing quality improvement.

SQE does this by authorizing all inspection procedures used throughout Intel's worldwide manufacturing facilities and providing technical support to the manufacturing sites. Because of its corporate status, SQE also provides trend analysis of cross-site supplier problems and quickly identifies the best supplier(s) for a certain part.

Specifically, SQE has five key responsibilities:

- 1) **Supplier qualification** through detailed surveys of suppliers' plants and processes.
- 2) **Continuing process quality improvement** through use of factory data and efforts to drive problem resolution back to the supplier level.
- 3) **Coordination, consultation & training** of Intel quality engineers through cross-site policies and procedures.
- 4) **Sustaining supplier quality** through active communications with suppliers on issues of quality and new technology, regularly scheduled quality improvement reviews, ongoing supplier audits and business reviews.
- 5) **New technology approvals.** SQE is responsible for assuring that all new technologies introduced into our purchased-materials base are at Intel-acceptable quality levels. SQE surveys, specifies and defines inspection criteria for new components being introduced into our manufacturing cycle.

**Systems Corporate Components Engineering (CCE)** qualifies all purchased commercial parts (or special variations of these parts) and develops any specialized tests required to inspect these parts prior to production use.

**System Peripherals and Power Supply Engineering (PPSE)** qualifies all peripherals (drives, CRTs, keyboards) and power supplies used in Intel products. PPSE writes the test program and develops any fixtures required to inspect these parts prior to production use.

**Design Engineering.** The design team originating a product is responsible for evaluating all Intel-designed parts — printed circuit boards, sheet metal, plastics, cables, etc. — going into that product.

#### **SITE MATERIALS QUALITY CHARTER**

Implementing SQE procedures at individual Intel sites is the responsibility of site-specific Materials Quality Engineering (MQE) groups. The MQE charter is to provide operational integrity within their plant area by providing problem analysis of plant-specific quality issues.



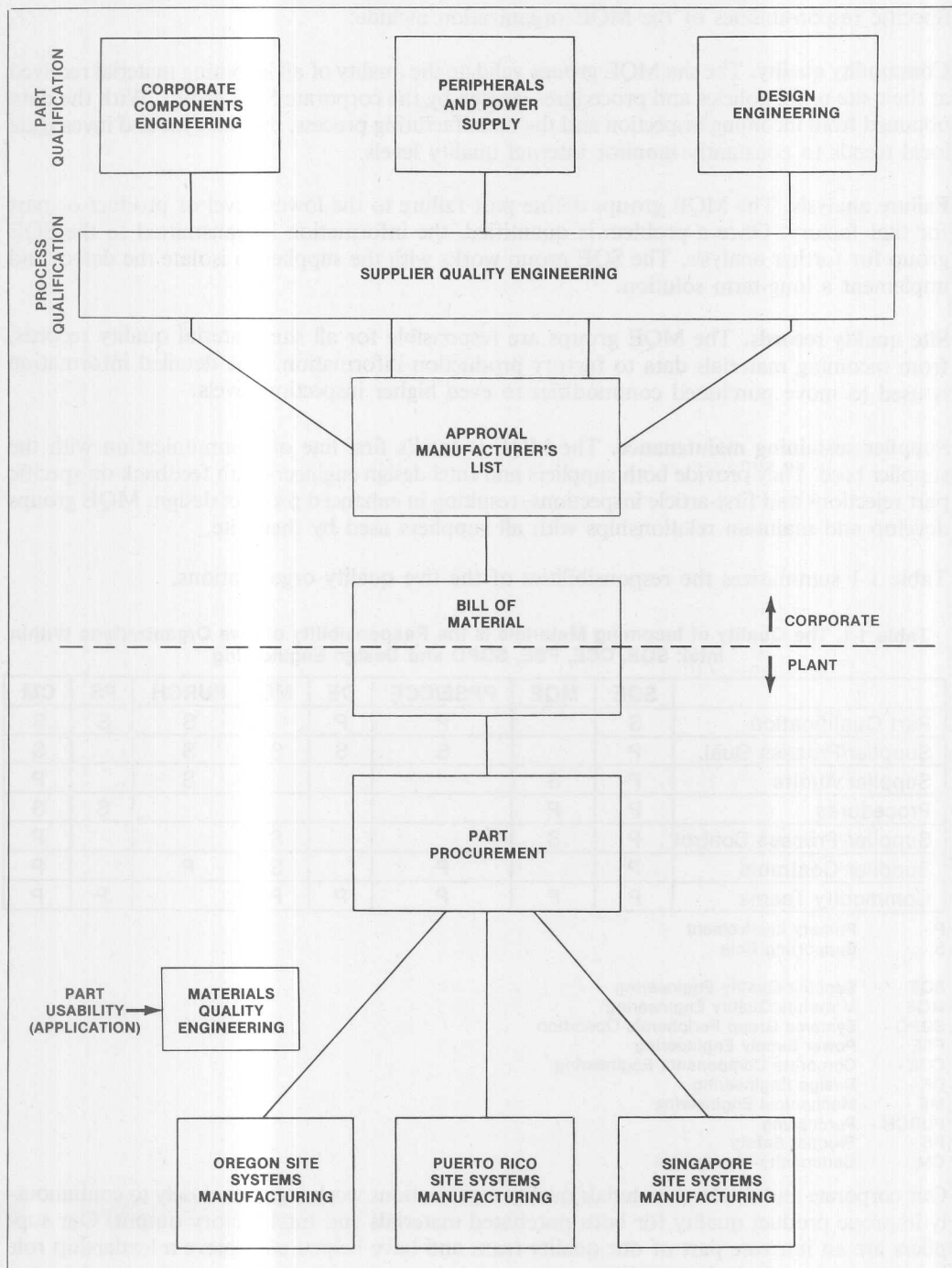


Figure 1-1. Intel's Materials Quality Program is Managed Cooperatively at Both Corporate and Plant Levels

Specific responsibilities of the MQE organization include:

**Commodity quality.** The site MQE groups validate the quality of all incoming material received at their site using policies and procedures written by the corporate SQE group. With the data obtained from incoming inspection and the manufacturing process, they analyze and investigate local trends to constantly monitor internal quality levels.

**Failure analysis.** The MQE groups define part failure to the lowest level of product or part for that factory. Once a problem is quantified, the information is transmitted to the SQE group for further analysis. The SQE group works with the supplier to isolate the defect and implement a long-term solution.

**Site quality records.** The MQE groups are responsible for all site material quality records, from incoming materials data to factory production information. The detailed information is used to move purchased commodities to even higher inspection levels.

**Supplier sustaining maintenance.** The MQE is Intel's first line of communication with the supplier base. They provide both suppliers and Intel design engineers with feedback on specific part rejections and first-article inspections, resulting in enhanced product design. MQE groups develop and maintain relationships with all suppliers used by their site.

Table 1-1 summarizes the responsibilities of the five quality organizations.

**Table 1-1. The Quality of Incoming Materials is the Responsibility of Five Organizations Within Intel: SQE, CCE, PSE, SGPO and Design Engineering**

	SQE	MQE	PPSE/CCE	DE	ME	PURCH	PS	CM
Part Qualification	S		P	P		S	S	S
Supplier/Process Qual.	P		S	S	S	S		S
Supplier Audits	P	S				S		P
Procedures	P	P					S	S
Supplier Process Control	P	S			S			P
Supplier Contracts	P		P		S	P		P
Commodity Teams	P	P	P	P	P		P	P

P - Primary Involvement  
S - Supporting Role

SQE - Supplier Quality Engineering  
MQE - Materials Quality Engineering  
SGPO - Systems Group Peripherals Operation  
PSE - Power Supply Engineering  
CCE - Corporate Components Engineering  
DE - Design Engineering  
ME - Mechanical Engineering  
PURCH - Purchasing  
PS - Product Safety  
CM - Commodity Management

Our corporate and site-level materials quality organizations work together closely to continuously improve product quality for both purchased materials and Intel factory output. Our suppliers are an intricate part of our quality team and have helped us achieve a leadership role in systems manufacturing quality.

### DOCK-TO-STOCK/JUST-IN-TIME MANUFACTURING

Intel's Systems Group supplier and parts quality programs are aimed at improving the quality of incoming materials to the point where Intel no longer needs to perform redundant quality inspections before moving parts to production. This objective has come to be known in the industry as Dock-to-Stock (DTS). Over 50 percent of our systems suppliers are currently at Dock-to-Stock inspection levels.

Once a supplier's quality and manufacturing systems control meet Intel's requirements, we work to establish delivery performance. The combination of DTS-level quality and predictable, reliable delivery constitute Just-in-Time (JIT) manufacturing, the ultimate goal at Intel.

The objective of JIT is to have the receipt of materials coincide with the time of use. This is accomplished by improving both the quality of incoming materials and the consistency of delivery to the point where only necessary materials are at the necessary place at the necessary time.

The JIT operational philosophy is the umbrella under which our quality program is run and, when fully realized, will allow us to completely eliminate the storage and inspection of incoming materials. See Figure 1-2, 1-3, and 1-4.

### COMMODITY MANAGEMENT

Prior to 1984, Intel's Materials Quality Group operated as a traditional quality control group, sampling and inspecting incoming shipments of material for conformance to specification. We recognized, however, that incoming and outgoing inspections were a "too-little, too-late" solution to the quality issue. To efficiently and repeatably turn out high-quality products, quality had to be built in at the point of manufacture.

With this in mind, we developed a new supplier methodology that requires a much closer working relationship between Intel and its suppliers. We call this program Commodity Management, and it requires a strong team effort by our Materials Quality, Purchasing, Engineering and Product Qualification Groups working with our supplier base. The Materials Purchasing organization supervises Intel's business relationship with suppliers. The Design Engineering and Qualification Engineering groups are responsible for defining material specifications.

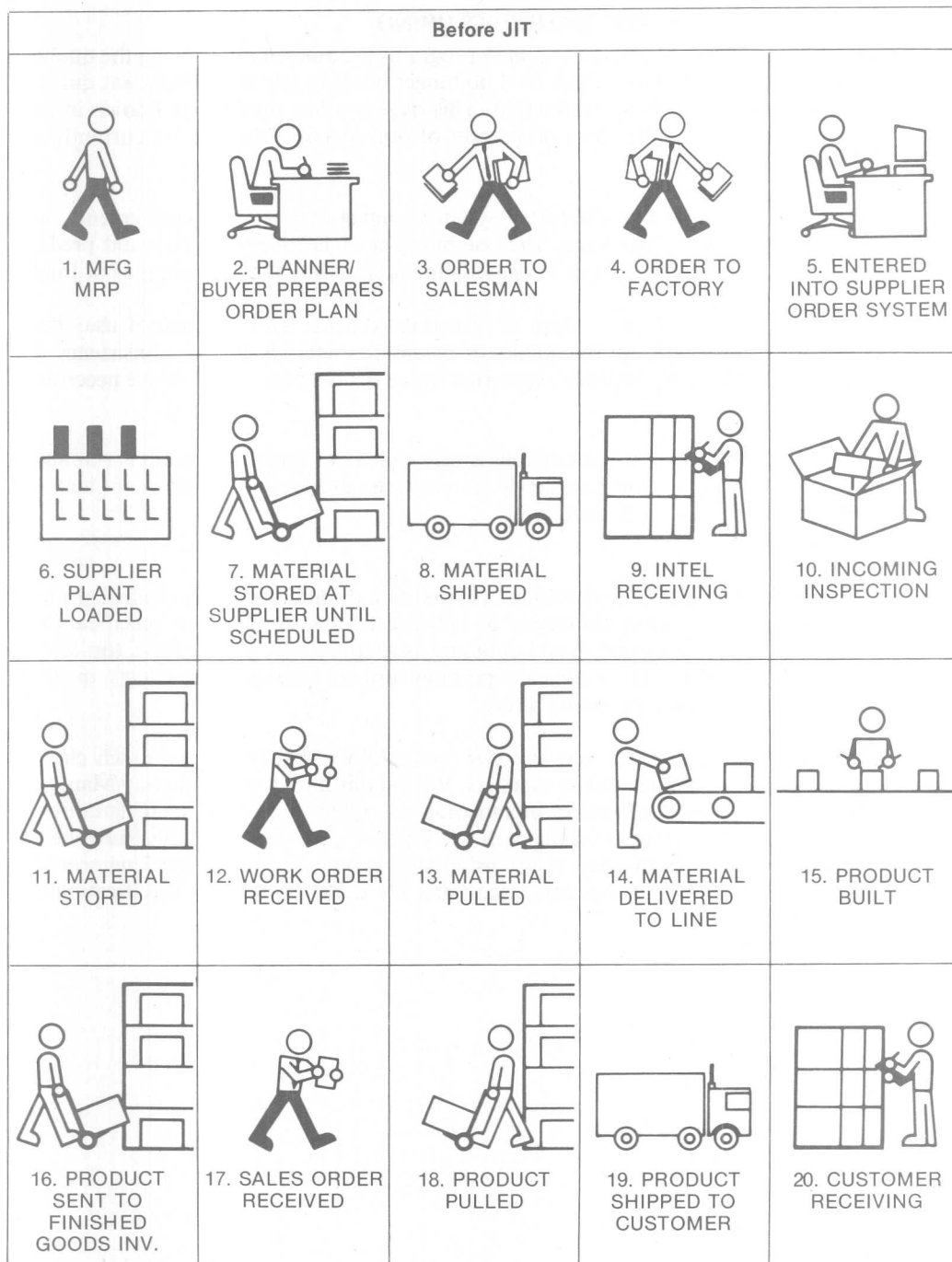


Figure 1-2. Before-JIT Manufacturing Environment



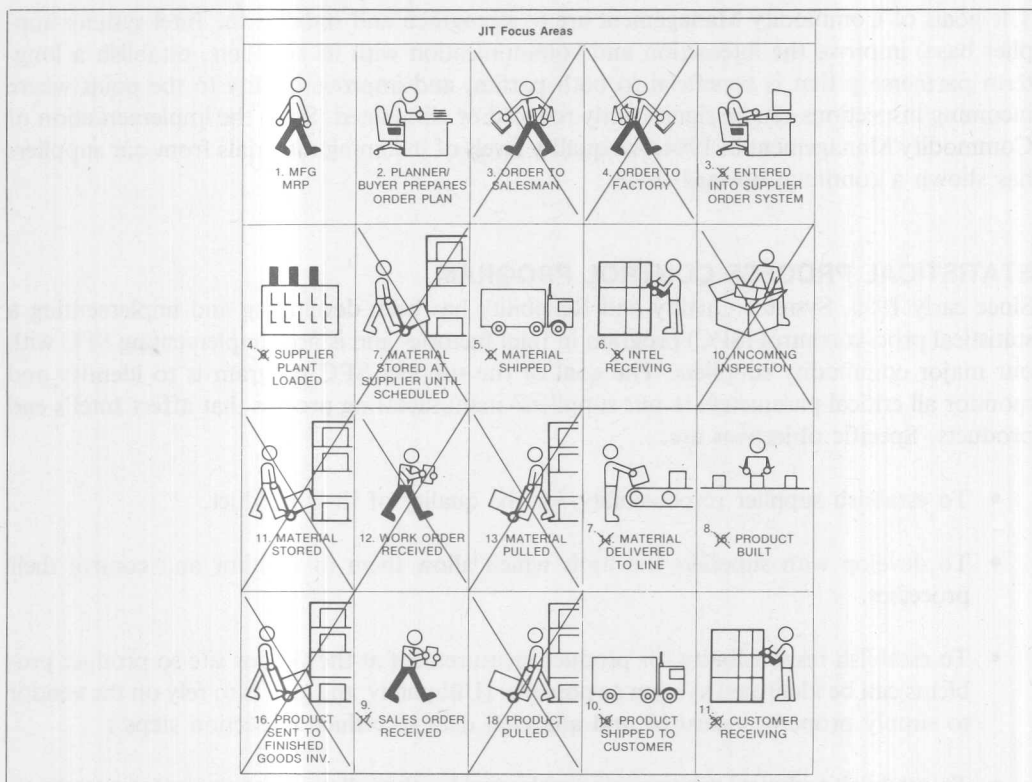


Figure 1-3. Flow Impacted by Implementation of JIT

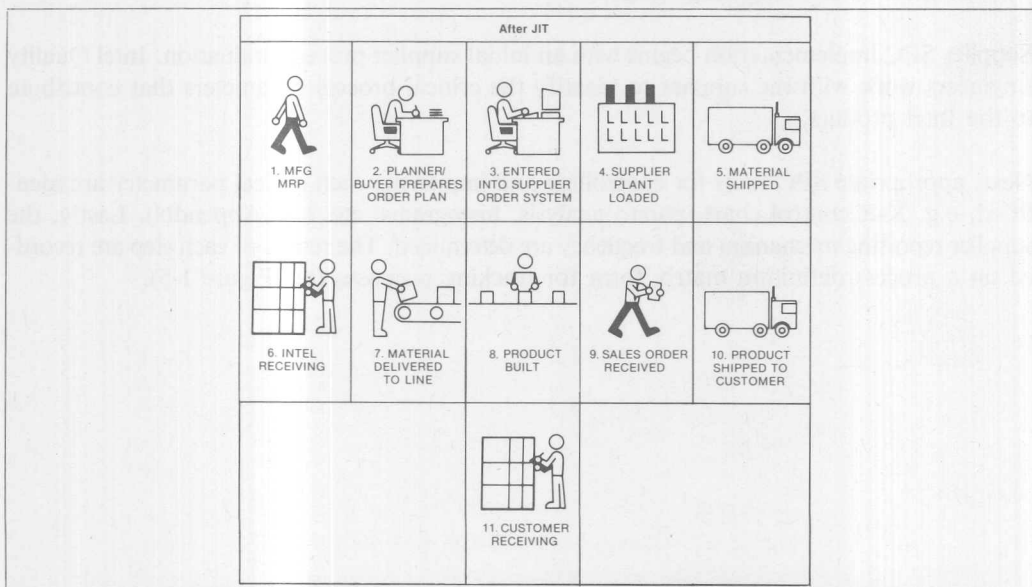


Figure 1-4. After-JIT Manufacturing Environment

The goals of Commodity Management are to strengthen and stabilize the Intel systems supplier base, improve the interaction and communication with its suppliers, establish a long-term partnership that is beneficial to both parties, and improve quality to the point where incoming inspections can be significantly reduced or eliminated. Since the implementation of Commodity Management in 1984, the quality levels of incoming materials from our suppliers has shown a continual upward trend.

### **STATISTICAL PROCESS CONTROL PROGRAM**

Since early 1985, Systems Quality and Reliability has been developing and implementing a statistical process control (SPC) program in Intel factories and is now implementing SPC with our major commodity suppliers. The goal of the supplier SPC program is to identify and monitor all critical parameters in our suppliers' manufacturing process that affect Intel's end products. Specific objectives are:

- To establish supplier responsibility for the quality of their product.
- To develop with suppliers the tools which allow them to monitor and control their processes.
- To establish responsibility for product measurement at the vendor site so product problems can be identified as soon as possible. (Ultimately, the goal is to rely on the vendor to supply properly measured and analyzed data to reduce inspection steps.)
- To establish technical relationships with vendors that allow them to improve products to meet Intel's long-range goals.

Supplier SPC implementation begins with an initial supplier process evaluation. Intel Quality Engineers work with the supplier to identify the critical process parameters that contribute to the Intel product.

Next, appropriate SPC tools for controlling and improving each critical parameter are identified, e.g.  $\bar{X}$ -R control chart, pareto analysis, histograms, etc. (see Appendix). Lastly, the supplier reporting mechanism and frequency are determined. The results of each step are recorded on a process definition matrix form for tracking purposes (see Figure 1-5).

PROCESS DEFINITION MATRIX				
Product: _____ Multilayer PWB _____		Supplier: _____		
Process: _____ Drilling _____		SQE: _____		
PROCESS CONTROL				
Process Parameter	Monitor/Control Tool	Sample Frequency	Process Specifications	Process Capability
1. Drill Speed/Feed	$\bar{X}$ -R Chart	1/5 Boards	60,000 $\pm$ 1,000 RPM*	Cpk $\geq$ 1.33
2. Retraction Speed	$\bar{X}$ -R Chart	1/5 Boards	1,000 $\pm$ 50 in./min.*	Cpk $\geq$ 1.33
3. Contact Head Pressure	$\bar{X}$ -R Chart	1/5 Boards	60 $\pm$ 2 PSI*	Cpk $\geq$ 1.33
Supplier Representative _____ Date _____		Intel Representative _____ Date _____		<b>Notes:</b> *Varies per chip load.

**Figure 1-5. Process Definition Matrix Form of Printed Wiring Board Drilling Process**

Once the process has been defined, a pilot evaluation is conducted to assess the effectiveness of the supplier's SPC program. This evaluation ascertains whether all critical parameters are operating in a state of statistical control and whether they meet Intel requirements. Upon successful completion of this evaluation the supplier becomes an Intel certified SPC supplier.

In addition to their SPC rating, suppliers are rated quantitatively on a number of other indices so vendors of "like" commodities can be easily compared. These indices include product quality, delivery, production performance and cost. The results influence the allocation of Intel purchases to suppliers by commodity management.

Figures 1-6 and 1-7 show the specific improvements Intel has realized in moving a particular commodity (incoming peripherals) to dock-to-stock status. Figure 1-8 shows our progress in moving our total supplier base to DTS status.

Specific benefits of Intel's Supplier SPC Program include:

- Reduction or elimination of incoming inspection (dock-to-stock)
- Reduction or elimination of outgoing supplier inspection or test
- Improved Intel manufacturing yields
- Improved supplier process yields
- Improved Intel product quality and reliability at substantially lower cost
- Decreased manpower allocated to the incoming inspection activity which, in turn, results in decreased material overhead costs

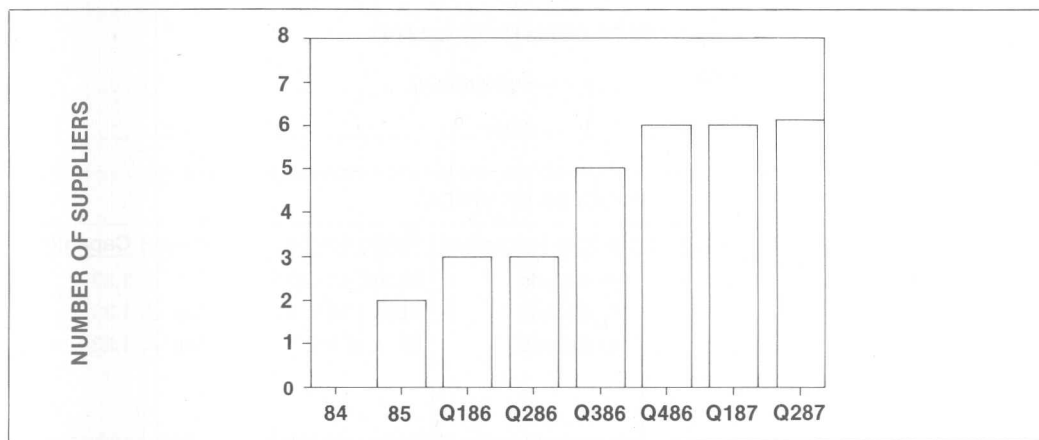


Figure 1-6. Intel Peripheral Suppliers Over Time. Showing Progress in Moving to Dock-To-Stock Status

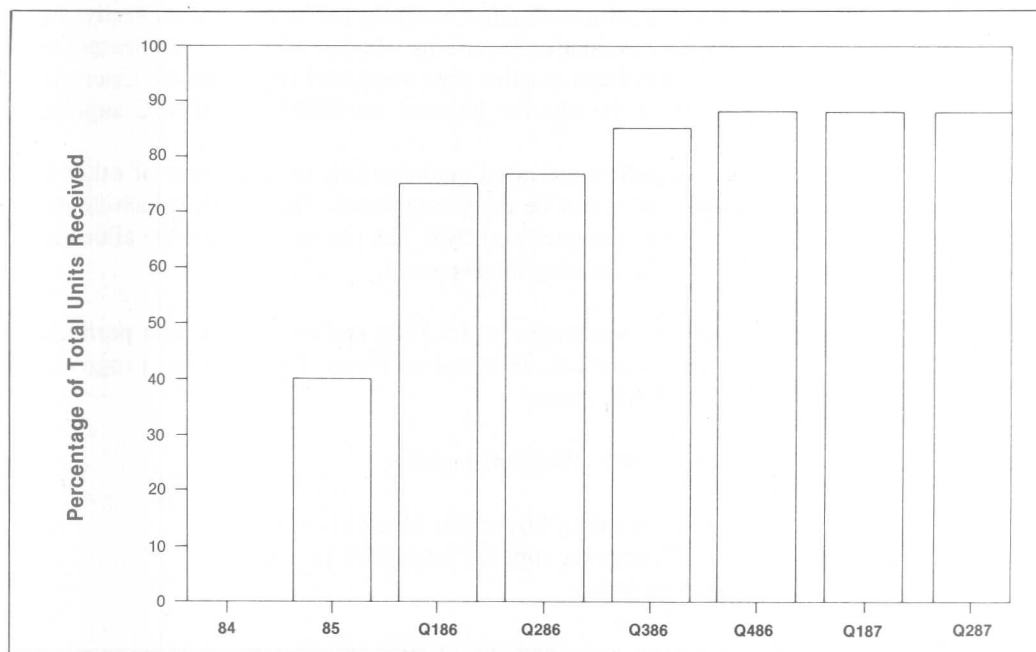


Figure 1-7. Percentage of Dock-To-Stock Peripherals Used in Intel Systems Manufacturing

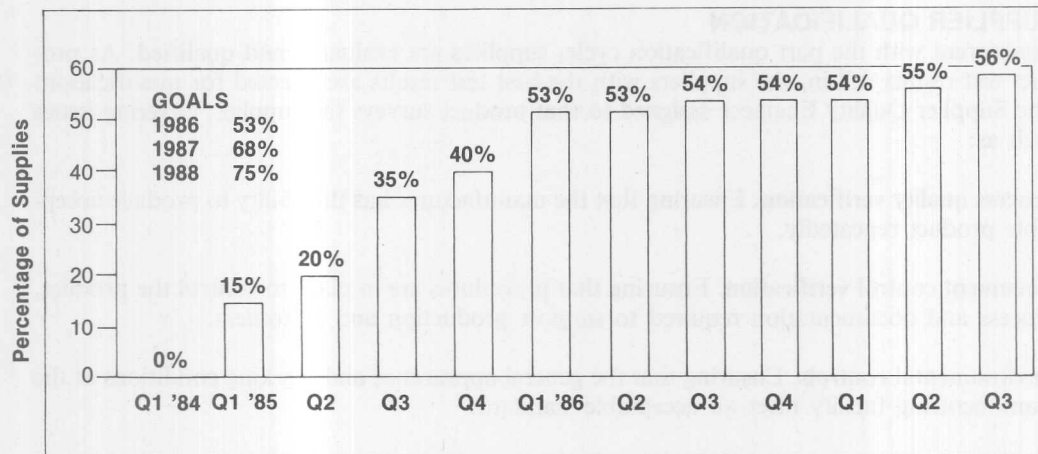


Figure 1-8. Total Intel Systems Supplier Base Over Time, Showing Progress in Moving Dock-To-Stock Status

### PART QUALIFICATION

Incoming materials are evaluated by one of four groups: Components Engineering (CCE), Peripherals and Power Supply Engineering (PPSE) or Design Engineering. The evaluation/qualification process is the same in all four groups, although the time involved at each step varies according to the commodity. Evaluation/qualification proceeds as follows:

**Preliminary Engineering Design.** First, a paper study is performed to ascertain availability of materials that meet the design.

**Part number assignment.** Next, the design engineer fills out a request for part number and contacts the appropriate qualifying group (CCE or PPSE). This group searches for a compatible or similar part already in the Intel documentation system. If none is found, they assign a new part number. Also during this stage, preliminary specifications are drawn up.

**Preliminary vendor selection.** After parts are assigned numbers and specifications are completed, Intel makes a preliminary survey of suppliers to determine which meet the design specifications.

**Sample parts procurement.** Samples of the selected parts are obtained from suppliers.

**Part tests.** The parts are tested and certified to meet both the manufacturer's and Intel's specifications. Any deviations must be resolved before qualification. If the part is qualified, incoming test inspections and production validation tests are designed for the part.

**Component part drawing (CPD) approval.** After the part is qualified and specifications are finalized, the Component Part Drawing (CPD) is signed and released for production.

**SUPPLIER QUALIFICATION**

Concurrent with the part qualification cycle, suppliers are evaluated and qualified. As product test results roll in, the suppliers with the best test results are selected for qualification. The Supplier Quality Engineer assigned to that product surveys the supplier, covering issues such as:

**Process quality verification.** Ensuring that the manufacturer has the ability to produce acceptable product repeatedly.

**Document control verification.** Ensuring that procedures are in place to control the product, process and documentation required to support production and customers.

**Environmental controls.** Ensuring that the general appearance and working conditions at the manufacturing facility meet an acceptable standard.

**Control of customer returns.** Ensuring that the supplier has materials review procedures in place and can perform failure analysis of customer-returned products.

**Training.** Training personnel in critical processes and hiring and replacing personnel.

A separate supplier survey procedure exists for every commodity purchased.

If a supplier passes both part qualification and plant and process qualification, he is approved as a supplier of that part for Intel and assigned "A" level status. That part can now be used throughout Intel Systems Group in any design. Figure 1-9 summarizes Intel's part and vendor qualification procedure.

**ONGOING MAINTENANCE OF PARTS AND SUPPLIER QUALITY**

When a supplier/part has attained "A" status, an audit plan is activated. This plan may vary in timing and depth for different commodities, but the steps followed are identical.

First, an audit procedure is established for each commodity. The procedure outlines the audit type and frequency for each supplier type, defines the tests and inspections to be performed on each part. Each part receives a periodic reinspection and audit to recertify the part as long as Intel uses it.

Suppliers are also reaudited, according to a specific procedure and on specified time intervals ranging from six to 24 months. In addition to the repeated audits, Intel arranges ongoing meetings with suppliers on a quarterly basis for the purpose of exchanging quality data and technology updates and performing business reviews.

All of these activities help build the Intel/supplier team, which is the key to ongoing success and continuing improvements in quality and performance.

**PURCHASED PRODUCT PROGRAMS**

Some Intel products are purchased from suppliers known as Outside Hardware Vendors (OHVs) and Outside Software Vendors (OSVs). An OHV is defined as a non-Intel facility manufacturing a board or system-level product for Intel. An OSV is a non-Intel facility designing, coding, testing, debugging, documenting and manufacturing a complete software product for Intel. Both are responsible for ensuring that all products are in full compliance with Intel functional, workmanship, quality, reliability and safety specifications. Normally, OHV/OSV products are marketed end-item products, requiring no Intel manufacturing contribution and are routed directly to the warehouse upon receipt.

The OHV/OSV program provides Intel with many benefits:

- It completes product niches that Intel cannot undertake due to engineering or manufacturing constraints
- It allows Intel to provide quick-to-market product strategies
- It allows Intel to leverage specific technologies or business expertise of the OHV/OSV
- It helps Intel provide a total-market solution for its customers

The program also benefits the OHV/OSV by allowing smaller companies to leverage Intel's marketing and after-sales support expertise.

**OHV/OSV Evaluation and Qualification**

Prior to becoming an Intel supplier, the OHV/OSV must be qualified. This qualification is based on a comprehensive evaluation synthesized from the supplier and manufacturing evaluation programs. Once qualified, the OHV/OSV must maintain its quality program to Intel standards.



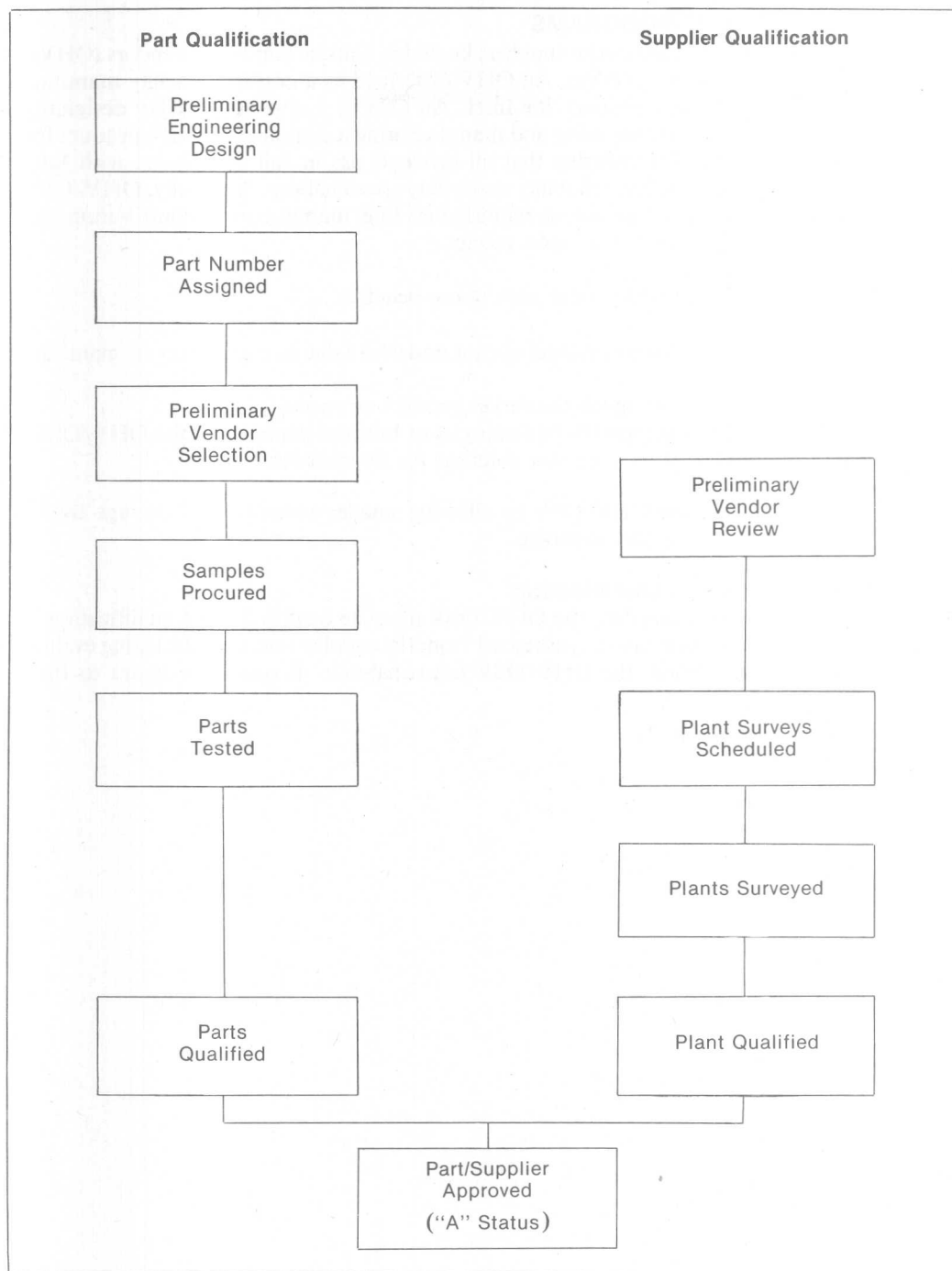


Figure 1-9. Flow Chart Summarizing Intel's Part and Vendor Qualification Procedures

**OHV/OSV Quality Assurance Program**

Due to the nature of OHV/OSV products—i.e., little or no value added by Intel—most quality assurance activities are focused on prevention. For example, an OHV is required to use statistical process control (SPC) methodologies in its manufacturing processes and to have an outgoing acceptance test procedure (ATP) to ensure adequate process and product controls. Similarly in the OSV program, quality assurance activities are focused on software development methodology and manufacturing (duplication). The OHV/OSV provides evidence of these controls by submitting SPC and ATP data to Intel on a monthly basis.

OHV/OSV conformance to Intel requirements is verified both through product acceptance testing and ongoing process audits. Process audits generally include but are not limited to the company's:

- Statistical process control (SPC) program
- Calibration control system
- Documentation control system
- Electrostatic discharge (ESD) control system
- Training program
- Preventive maintenance program
- Product acceptance test procedure (ATP)
- Failure analysis and customer return program

The OHV/OSV is also contractually required to provide complete traceability of OHV/OSV products through a product-specific serialization system and to include Intel in the approval process for all product revisions affecting product form, function or fit.

**OHV Product Reliability**

OHV products mean time between failure (MTBF) requirements are based on MIL-STD-217D calculations. Since these are generally considered conservative estimates, the actual MTBF is determined through life-test demonstrations. Ongoing reliability evaluation occurs through analysis of field failure/customer return data.

**OHV Product Regulation**

The OHV is contractually required to certify its product for safety, environmental and regulatory specifications such as Underwriters Laboratories, the Canadian Standards Association, the Federal Communications Commission and Technischer Überwachungs-Verein (TUV). On request, Intel may assist the OHV by allowing them to use Intel's environmental laboratory, Intel product safety engineers, etc. Regardless of the level of Intel participation, the OHV is solely responsible for securing all necessary product certifications.

**Quality and Reliability Contractual Requirements**

An Intel quality engineer participates in all OHV/OSV contract negotiations and is responsible for assuring quality, reliability and safety terms and conditions are in the contract. These terms and conditions include both general OHV/OSV and product-specific quality/reliability/safety requirements. See Figure 1-10.

**ATTACHMENT "A"****1.0 Minimum Acceptable Quality Levels for OHV products:****1.1 For 19\_\_\_\_\_****1.1.1 Minimum Acceptable FPA:**

Electrical	_____	DPM
Mechanical	_____	DPM
Cosmetic	_____	DPM
Administrative	_____	DPM

Overall Acceptable Quality: \_\_\_\_\_%

**1.1.2. Maximum Acceptable DOA: \_\_\_\_\_% confirmed.****1.2 For 19\_\_\_\_\_****1.2.1. Minimum acceptable FPA:**

Electrical	_____	DPM
Mechanical	_____	DPM
Cosmetic	_____	DPM
Administrative	_____	DPM

Overall Acceptable Quality: \_\_\_\_\_%

**1.2.2. Maximum Acceptable DOA: \_\_\_\_\_% confirmed.****1.3 For 19\_\_\_\_\_****1.3.1. Minimum acceptable FPA:**

Electrical	_____	DPM
Mechanical	_____	DPM
Cosmetic	_____	DPM
Administrative	_____	DPM

Overall Acceptable Quality: \_\_\_\_\_%

**1.3.2. Maximum Acceptable DOA: \_\_\_\_\_% confirmed.****2.0 Minimum Acceptable Reliability:**

**2.1** Mean Time Between Failures (MTBF) requirement is \_\_\_\_\_, \_\_\_\_\_ hours at 60% confidence level throughout the operating range of the product.

**2.2** This figure shall be demonstrated via calculation and by using an actual life test set-up.

**Figure 1-10. Sample OHV Quality and Reliability Contractual Terms and Conditions****MATERIALS QUALITY INSPECTION**

Incoming inspection has been the traditional gate used to measure vendor quality and to protect manufacturing lines from low-quality material. At Intel, Systems Quality and Reliability has modified that tradition by working with suppliers to assure that parts are of production-line quality when delivered to Intel. However, until full DTS status is achieved throughout our own and our suppliers' factories, we will continue to rely on incoming inspections to ensure appropriate quality levels for all parts going into Intel Systems products.

The Systems Quality Engineering (SQE) group is responsible for designing and developing new inspection techniques, for researching and qualifying new Intel suppliers and for determining inspection requirements.

The site-level Materials Quality Engineering (MQE) groups are responsible for implementing these quality procedures by inspecting incoming materials and auditing supplier quality.

Inspection procedures are based on four categories (all products may not be required to go through all four procedures):

- Visual inspection
- Dimensional inspection
- Electrical/functional testing
- Special inspections

Visual inspection looks for deviations from normal product appearance, changes or inhomogenities in color, physical blemishes or defects, mismarking, etc. While visual defects may not always result in product malfunction, Intel Quality operates under the philosophy that products without visual flaws are often of better production quality than products with visual flaws.

Dimensional inspection is more quantifiable. All purchased commodities reference a specific set of Intel drawings. Dimensional inspection is required since form, fit or function of a product may be adversely affected by inadequate dimensional control.

Electrical/functional test is the most detailed of the inspections and is used to test the most complex incoming products. Power supplies, peripherals, and some components are tested electrically; however, Intel attempts to drive this test back to the supplier level so that products pass complete electrical inspection prior to shipment.

Special inspections are product-specific inspections such as solder tests on printed wiring boards.

During inspection, reject lots or defective parts are occasionally encountered. When this happens, an Intel Material Review Board reviews the rejection and either returns the material to the supplier; destroys the flawed parts; uses the parts if they do not impact form, fit or function; or reworks the parts until they are acceptable for production.

### **Material Quality Evolution**

As the quality of incoming material improves, we move towards full Dock-to-Stock manufacturing status. In the process, a part/product moves through four inspection levels:

- 100% inspection
- Skip lot
- DTS (Dock-To-Stock)
- DTL (Dock-To-Line)

**100% Inspection.** 100% inspection is the most stringent of all inspection levels. When parts are received they are subjected to a first-article inspection with very detailed measurements. Deviations are noted and resolved either through modifications by the supplier or specification changes.

Precise inspection records are maintained for each lot of material received, including lot size, sample size, date received, date inspected, lot number and purchase order number (see Figures 1-11 and 1-12).

**Skip Lot.** As quality increases, the part moves to the next level called “skip lot,” a minimum inspection of ten consecutive lots with no rejections. Skip lot means every other lot bypasses inspection and goes directly to inventory. A lot rejection at this stage, however, causes the status to return to a 100% inspection basis.

Moving to the skip lot level of inspection requires conformance to Intel’s Inspection Level Change Request Procedure #187365, shown in Figure 1-13.

**DTS (Dock-To-Stock).** For a product to proceed directly from the loading dock to inventory without inspection, a minimum of five lots must have passed through Incoming Quality Assurance (IQA) at the skip lot level with no rejections in either IQA or on the production floor.

**DTL (Dock-To-Line).** The ultimate quality status for incoming products is called Dock-To-Line (DTL) and has materials flowing from the receiving dock directly to the production line. DTL status designates not only a quality product but on-time delivery. DTL eliminates IQA and inventory and is the full accomplishment of Just-In-Time manufacturing.

Parts at all inspection levels are periodically audited by pulling random samples for inspection and test. A random audit failure can result in degradation of the product’s/supplier’s inspection status.

## **MATERIALS FLOW CONTROL**

### **Planning and Purchasing**

Supporting Intel’s corporate-wide quality control program is a sophisticated, comprehensive materials ordering and inventory control system called the Intel Manufacturing/Materials Automated Control System (iMACS). iMACS integrates all Systems Group inventory, bills of material, Manufacturing Resource Planning and factory control data to provide comprehensive control of Intel’s System Group material planning, purchasing and inventory. All “A” status parts are logged in iMACS, allowing world-wide Systems manufacturing sites to coordinate their ordering and stocking practices.

Quality is also factored into Intel’s long-range product plans. The SQEs, planning and purchasing and the commodity teams develop five-year business plans for all major commodities. These plans, called Material Long Range Plans (MLRP’s), provide a comprehensive look at Intel’s product direction in light of the commodity’s industry-wide direction and merge this

Figure 1-11. Sample Lot History Card from Intel Inspection Records

VARIABLES CONTROL CHART ( $\bar{X}$  & R)

VARIABLES CONTROL CHART (X & R)																								GOLD THICKNESS				CHART NO.	
SUPPLIER												NON-FIRST ARTICLE OR ENGINEERING												SPECIFICATION LIMITS .00003 MIN.					
MACHINE MICRODEERM												GAGE				UNIT OF MEASURE MICROINCHES													
DATE		5-15-86				5-15-86				5-16-86				5-22-86				5-29-86				6-27-86							
TIME				→ 3:10				→ 2:45				→ 12:15				→ 7:35				→ 8:05									
SAMPLE MEASUREMENTS	1	44	33	30	37	30	34	30	30	31	34	30	54	36	48	37	32	30	33	55	37	31	37	32					
	2	39	33	34	33	30	36	36	31	32	37	31	36	47	38	47	35	34	30	33	34	30	33	33					
	3	36	35	36	30	35	36	40	30	34	32	33	34	48	39	55	34	30	34	36	45	34	33	34					
	4	39	35	31	33	39	46	31	31	30	34	31	51	36	39	55	40	32	30	33	46	35	34	37					
	5	44	36	34	41	39	41	35	37	30	32	30	51	38	48	42	31	31	37	35	34	31	38	31					
SUM		202	172	165	174	173	193	172	159	157	169	155	226	205	212	236	172	157	164	192	196	161	175	167					
AVERAGE, $\bar{x}$		40.4	34.4	33.0	34.8	34.6	38.6	34.4	31.8	31.4	33.8	31.0	45.2	41.0	42.4	47.2	34.4	31.4	32.8	38.4	39.2	32.2	35.0	33.4					
RANGE, R		8	3	6	11	9	12	10	7	4	5	3	20	12	10	18	9	4	7	22	12	5	5	6					
NOTES																													





## Procedures

REV. 1

NO. 187365

PAGE 12 OF 13

TITLE: INTEL REQUIREMENTS FOR CHANGES IN INSPECTION LEVELS PROCEDURE 7 SQP 3.17

## ATTACHMENT "A"

## INSPECTION LEVEL CHANGE REQUEST

See Procedure 187365 "INTEL REQUIREMENTS FOR CHANGES IN INSPECTION LEVELS" section 5.0 for instructions in filling out this form.

1. ORIGINATOR: \_\_\_\_\_ 2. DATE: \_\_\_\_\_ 3. MAILSTOP: \_\_\_\_\_
  4. INTEL PART NUMBER: \_\_\_\_\_ REVISION LEVEL: \_\_\_\_\_
  5. MANUFACTURER: \_\_\_\_\_
  6. MANUFACTURER PART NUMBER: \_\_\_\_\_
  7. PRESENT INSPECTION LEVEL: 100% SAMPLE: SKIP LOT: DOCK-TO-STOCK/LINE BREADMAN \_\_\_\_\_
  8. REQUESTED INSPECTION LEVEL: 100% \_\_\_\_\_ SAMPLE: \_\_\_\_\_ SKIP LOT: \_\_\_\_\_ DOCK-TO-STOCK/LINE \_\_\_\_\_ BREADMAN \_\_\_\_\_
  9. WHAT IS THE REASON FOR REQUESTING CHANGE IN INSPECTION LEVEL?
    - A. Meets Sec. 4.1 Requirements \_\_\_\_\_; Attach copy of Lot History Card
    - B. Rejected lot in IQC \_\_\_\_\_; Attach copy of Rejected Report
    - C. Factory Failure Rate \_\_\_\_\_; Attach Supporting Data Reports
    - D. Purge \_\_\_\_\_; Attach copy of Purge Notice
    - E. Change in item number rev level; Attach copies of previous authorized ILCR's.
    - F. Other \_\_\_\_\_; Attach explanation.
  10. Average Factory Performance as directly related to Incoming Material Quality (in DPM) \_\_\_\_\_; if available.
  11. Additional information and comments; attach documentation if necessary.  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_
  12. SIGN OFF: \_\_\_\_\_ DATE: \_\_\_\_\_  
Originator: \_\_\_\_\_  
MQE \_\_\_\_\_
  13. As the Manufacturing Site Representative I Approve/Disapprove (circle one) this request to change the Inspection Level based on Factory Performance of this specific Supplier Item Number.  
QE/TE/ME/PE Manager: \_\_\_\_\_ Date: \_\_\_\_\_
  14. As the Corporate Representative for Intel Systems Quality I Approve/Disapprove (circle one) this Inspection Level Change Request.  
SQE \_\_\_\_\_ Date: \_\_\_\_\_
- CC: IQC Part number file  
Originator  
Site ME/PE/QE/TE Manager  
SQE (Corporate)  
MQE (Sites)  
Purchasing Manager (Sites)  
Material Control Manager (Sites)  
AML Data Entry
- ATTACHMENTS: (Required at final approval)
- Lot History Card (copy from all using sites).
  - Reject Data as Appropriate
    - IQC
    - Factory
    - Field
    - Purge Notice

Figure 1-13. Inspection Level Change Request Form

information to give a strategic direction for Intel within that commodity area. MLRP's are updated annually.

### Approved Manufacturers List (AML)

All parts approved for use in Systems Group products are controlled by a computerized list detailing part/vendor relationships. This listing, called the Approved Manufacturers List (AML), contains the specific part number, vendor relationship and numerous codes that quantify the inspection levels used at Intel (see Table 1-2). A supplier must be "A" status or better to be used unconditionally in Intel production.

**Table 1-2. Intel Approved Manufacturers List**

AMLOR030C DATA DATE 7/1/86 REQUESTOR ID										INTEL CORPORATION APPROVED ITEMS LIST SEQ BY PC—CODE, ITEM NUMBER		
Confidential			C C	C	T C		AI			S		
		R	O O	N	Y O		UN			T	S	
Intel Item Number		E	M D	T	P D	SUB- COMM	TS OT	OWN	Description	A	P	Manufacturer Name
123456-001		V	M E	L	E E	2190	N	090	Capacitor	A		ABC Corporation 111 North Street Portland, Ore
234567-001	01		2 1	D	7 1	2190	N	090	IC, 74LS001	A		XYZ Corporation 222 South Street Portland, Ore
345678-001			2 1	D	7 1	2190	N	090	Resistor	A		TUD Corporation 333 East Street Portland, Ore

Each part number in Intel's production system has a specific vendor associated with it. iM-ACS and the AML are tied together electronically, preventing purchase orders from being issued to suppliers not authorized to provide these parts.

### CONCLUSION

The Systems materials quality team — Supplier Quality Engineering, Corporate Component Engineering, Peripherals and Power Supply Engineering and Systems Reliability Engineering — working in concert with our suppliers, has made significant strides in improving the quality of incoming materials at Intel. Over 50% of our suppliers are at dock-to-stock or better inspection levels.

Our supplier statistical process control (SPC) program continues to generate improvements in purchased materials, resulting in improved product reliability. It also will continue to improve process controls which allow repeatability and consistency in both product and delivery.

Continuing teamwork between Intel and its suppliers is the cornerstone of long-term quality improvement.





## **CHAPTER 2 RELIABILITY**

### **INTRODUCTION**

Throughout the growth of our product line, Intel has led its markets in product reliability while providing leading-edge microprocessor technology in both single-board computers and microprocessor systems. Our success is based on a simple formula: develop the product with reliability in the design, manufacture the product with stringent process control and continually audit the product both in the factory and in the field.

With numerous engineering departments and the technologically complex products, it is important to develop consistent reliability practices. To bring direction and control to the reliability effort, Intel established Systems Reliability Engineering (SRE). This group is chartered with providing and managing the systems group reliability program. This is accomplished by SRE focusing on the following areas:

- Reliability program policies and procedures
- Laboratory facilities and testing
- Reliability training and communication
- Reliability qualification of new technology
- Program conformance monitoring

### **RELIABILITY PROGRAM**

Nine documents define Intel's system reliability program. The first document is a policy that defines the need for a reliability program and the responsibilities for implementing that program. The remaining eight documents are procedures that describe the methodology of performing specific reliability activities. The proceduralized reliability activities are:

- Reliability Specification Procedure
- Reliability Plan Procedure
- Derating Procedure
- Component Failure Rate Estimation Procedure
- MTBF Prediction Procedure
- Reliability Testing Procedure
- Reliability Report Procedure
- Audit Kit Procedure

### **RELIABILITY SPECIFICATION**

During product proposal, the reliability requirements for the product are defined in the reliability specification. Reliability requirements are:

- Environmental definition (temperature etc.)
- Component derating requirements

- Duty cycle (disk drives etc.)
- Fault tolerant capabilities
- MTBF requirement (and MTBF apportionment for systems)

### RELIABILITY PLAN

Upon completion of the design feasibility study, the project enters a formal design phase. At the onset of the design phase the reliability plan is written. The reliability plan describes the reliability activities to take place from design to manufacturing. Standard activities to ensure reliability are:

- Component selection review
- MTBF prediction
- Design review
- Functional evaluation
- Thermal and air flow analysis
- Environmental stress testing
- Reliability test
- Failure analysis
- Corrective action
- Reliability report

### MTBF PREDICTION

A predicted mean-time-between-failure (MTBF) is calculated early in the design stage to determine if the product will meet its reliability criteria. The MTBF prediction, a paper calculation, is also used to identify any potential weak links within the product and serve as a guide for the reliability demonstration test. In calculating an MTBF prediction, information required is:

- Component failure rates (at temperature)
- Structure model (series, parallel)
- Duty Cycle

Component failure rates are obtained from multiple sources. For all Intel components, in-house demonstrated failure rates are used. These failure rates are obtained from the component reliability groups and are quoted as Fit values (failures per  $10^9$  hours) at 55°C and 60% confidence level. For non-Intel components, component failure rates are calculated in accordance to a Bell Communications Procedure that currently models components failure rates more closely to Intel's semiconductor experience than MIL-HDBK 217E.

For a system that has a constant failure rate and a series non-redundant design (if any one component fails, the whole system fails), the predicted MTBF is the reciprocal of the sum of the individual failure rates.

$$mtbf = \frac{1}{\sum_{i=1}^n \lambda_i}$$

mtbf = mean time between failure

$\lambda_i$  = failure rate of each component

example:  $\lambda_1 = 4.5 \times 10^{-6}$

$\lambda_2 = 2.0 \times 10^{-6}$

$\lambda_3 = 7.5 \times 10^{-6}$

$$mtbf = \frac{1}{(4.5 + 2.0 + 7.5) \times 10^{-6}} = 71,429 \text{ hours}$$

In a system-level MTBF prediction, it is important to incorporate duty cycle for disk drives, streamer tape, keyboards and printers. Duty cycle is used for devices (typically electromechanical) that are not actuated 100 percent of the time.

For example, a disk drive will have one failure rate associated when making drive accesses (reading or writing) and a second failure rate when idle (not accessing). If the user's application is limited disk drive accesses, the overall drive failure rate is low. However, if the user's application involves continuous disk drive accesses, the overall disk drive failure rate is higher and the system MTBF is lower.

An example below shows a duty cycle calculation for an electromechanical device that is to be included in an MTBF prediction.

example:

$mtbf_{\text{running}} = 10,000 \text{ hours and } 25\% \text{ duty cycle usage } (DC_r = .25)$

$mtbf_{\text{idle}} = 100,000 \text{ hours and } 75\% \text{ duty cycle usage } (DC_i = .75)$

$$mtbf = \frac{1}{DC_{\text{running}} (\lambda_r) + DC_{\text{idle}} (\lambda_i)}$$

$$mtbf = \frac{1}{.25 (1/10,000) + .75 (1/100,000)}$$

$$mtbf = 30,769 \text{ hours}$$

## RELIABILITY BATHTUB CURVE REVIEW

It is the purpose of the reliability test to show rate of failure over time. Three characteristic curves are used in reliability to describe component and system failure rate as a function of time. These characteristic curves are the early failure rate curve, the random failure rate curve and the wearout failure rate curve. Each curve provides a continuous measurement of failure rate  $\lambda$  (lambda) over time and is associated with a different time-dependent failure mode distribution.



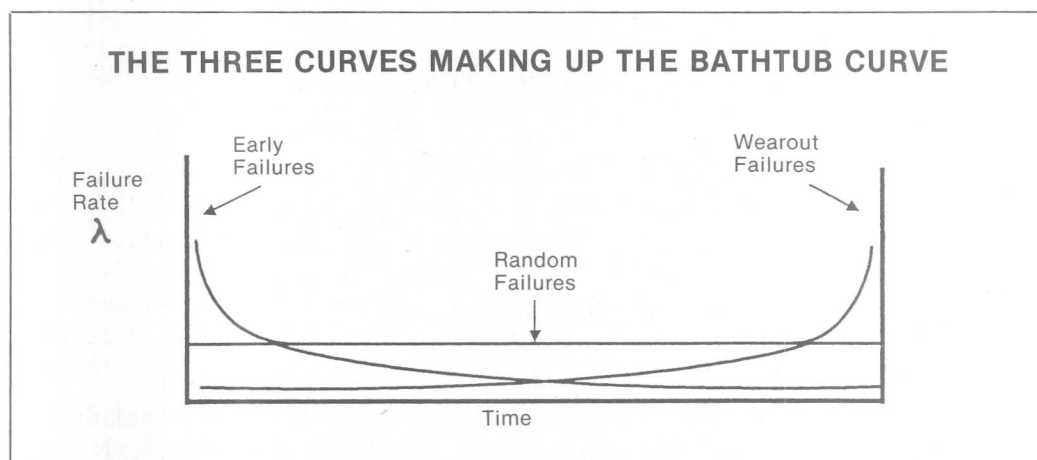


Figure 2-1. The summation of these three curves yields the bathtub curve.

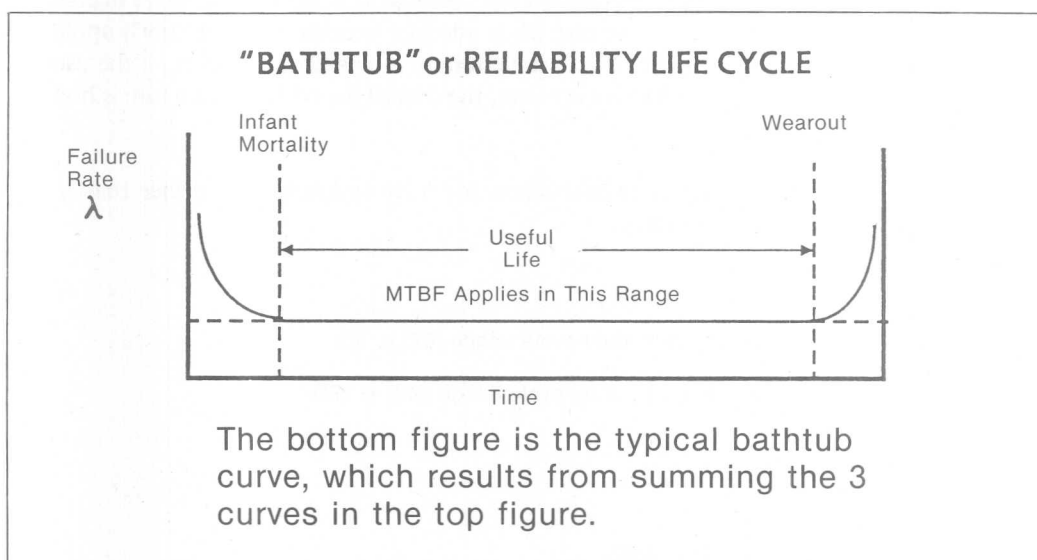


Figure 2-2. The bathtub curve has three distinct regions; infant mortality, useful life and wearout.

The infant mortality region is due to early failures that are a result of substandard material control or process deficiencies. The early failure rate curve is characterized by a decreasing failure rate over time.

The useful life region is the flat portion of the curve between the infant mortality region and the wearout region. This part of the bathtub curve is due predominantly to random failures which are modeled by the exponential probability distribution. During this period of constant failure rate  $\lambda$ , the reciprocal of the failure rate is equal to the MTBF.

The useful life region is terminated by the onset of wearout. Wearout is characterized by an increasing failure rate over time. For system products, electromechanical devices such as switches, rotating memory, fans and batteries are typical causes of wearout failures.

### RELIABILITY TESTING

Intel performs an MTBF demonstration test on all new products before they are released for final production. Products tested are from the early production run and have undergone all manufacturing process steps. All units are representative of what we deliver to our customers.

Reliability testing is performed in the reliability lab, where there are dedicated chambers for long-term board testing and walk-in ovens for system testing. All testing is done at the products' upper operating temperature limit; for boards, this is typically 55°C and for systems 40°C.

During the reliability test, the units under test are functionally operated to simulate a true user environment. There is also an independent development cycle for the reliability test software and any required support hardware.



Figure 2-3. Reliability Laboratory

### Reliability Test Preparation

Prior to the start of the reliability test, the reliability test chamber is characterized for proper operation under thermal load and air flow. The chamber is then fitted with appropriate card cages, fans, wire harnesses and external power supplies. Backplanes are inspected for clean contacts; cables and boards are checked for proper seating; and external disk drive heads are cleaned at test start and periodically thereafter according to the maintenance schedule. After power-on, the power supplies are then checked for nominal voltage at the backplane. Additionally, the AC power line is externally monitored to log any power failure or on-line voltage conditions that may occur.

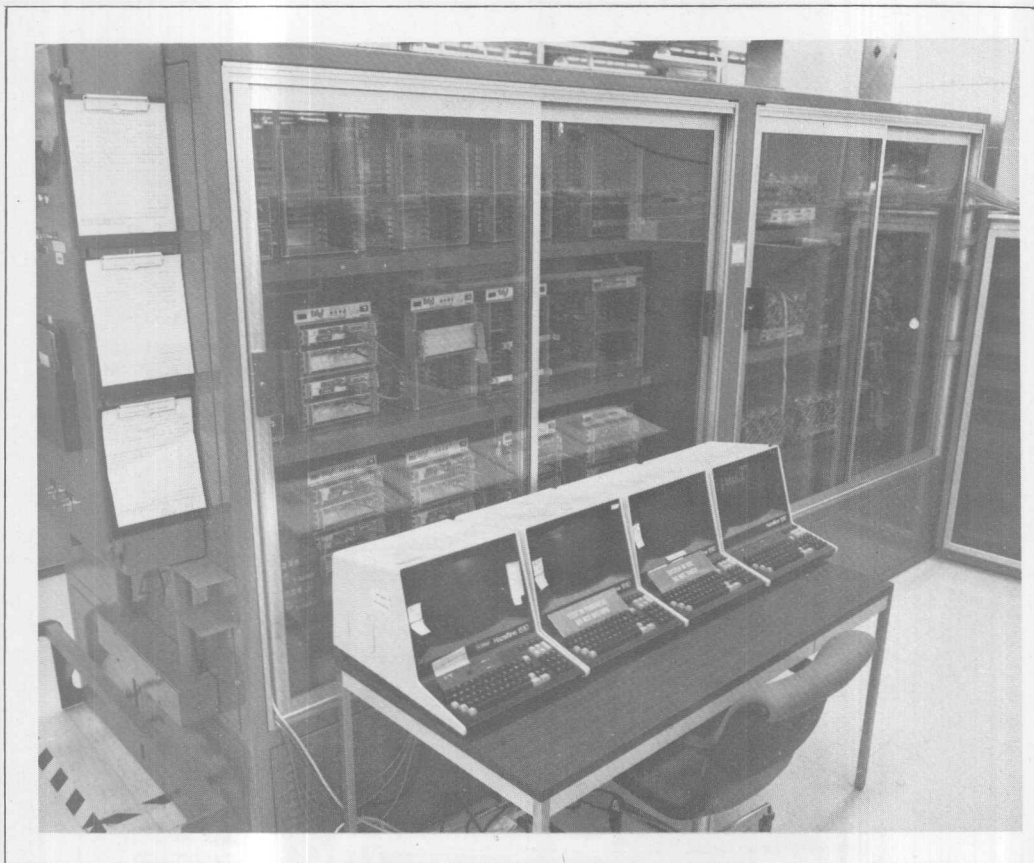
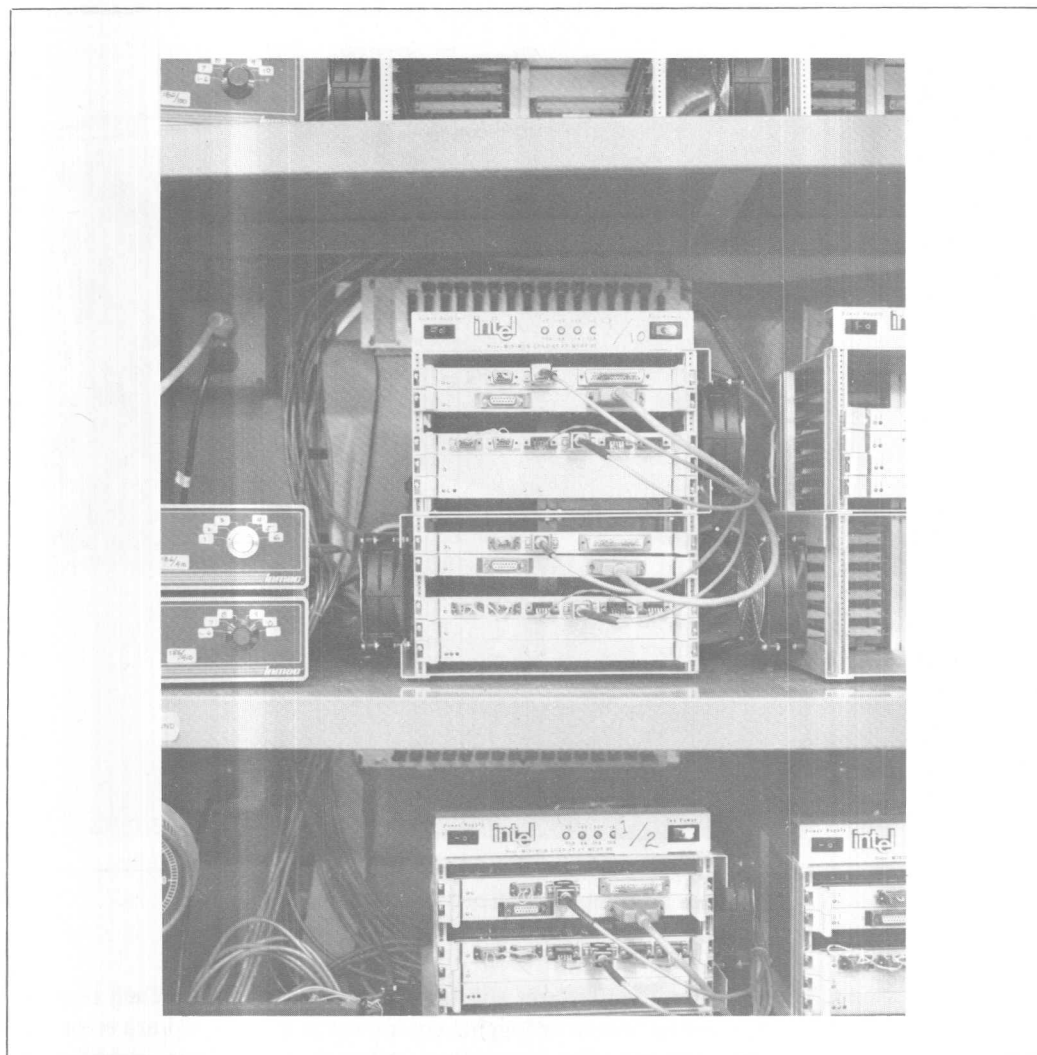


Figure 2-4. Reliability Board Test Chamber

### Data Logging

During the reliability test, intermittent failures and hard failures may occur. When possible, external real-time data monitoring and error logging equipment is used to capture error data and status information for each unit under test. Data collected includes unit identification number, time of failure, number of successful passes before failure, test type failed and error status information.



**Figure 2-5. Reliability Testing of MultiBus® II Boards**

### **Failure Analysis and Corrective Action**

During the course of the reliability test, failures that occur receive full investigation. Failure analysis investigation may yield a system-level, board-level or component-level failure mechanism. Intermittent failures are the most difficult to track down. Classification of failures include:

- Hard failures - occurs repeatedly despite power cycling or reset
- Intermittent failure - disappears randomly or upon power cycling or reset
- External failure - external causes, not due to unit under test

After failure investigation, if corrective action is applied and successfully verified, then the failure is censored and not counted against the MTBF. If an intermittent failure occurs and cannot be isolated, worst case is assumed, and it is counted against the MTBF. A failure due to verifiable external causes, such as power line interruption, would not be counted against the MTBF.

In the failure analysis process, if the component failure mechanism cannot be determined externally, the component is then decapsulated for analysis. A table of MOS device failure mechanism is shown:

**Table 2-1. MOS Device Failure Modes**

Failure Mode	Activation Energy ( $E_a$ )	Detection	Prevention
Oxide defects	0.3 eV	High voltage operating	Ultra-clean processing and high-voltage stress screens
Refresh Degradation	0.5 eV	High temp bias	Ultra-clean processing
Contamination	1.0 eV	High temp bias	Ultra-clean processing, guard rings
Silicon Defects	0.5 eV	High voltage cell stress and guardbanded tests	Quality control and ultra-clean processing and high-voltage stress screens
Metal Line Electromigration	0.5 eV	High temp operating life	Optimal design rules, process control
Contact Electromigration	0.9 eV	High temp operating life	Optimal design rules, processing control
Masking defects/ Assembly defects	0.5 eV-1.0 eV	High temp storage and	Quality control, inspection
Microcracks	N/A	Temp cycling	Optional design, low stress packaging, low film stresses
Short Channel Charge Trapping	-0.06 eV	Low temp. high voltage operating life	Optimal transistor design, high quality oxide, process control
Soft Error	N/A	Low voltage operation and accelerated alpha source	Optimal design, material quality, process control

## RELIABILITY REPORT

A reliability report is written after the completion of the reliability demonstration test. Included are all qualification activities from design to manufacturing. One of the most important sections in the reliability report is the reliability demonstration test results. This contains reliability test hour temperature conversion, the point estimate MTBF and the 60 percent confidence limit.

## Acceleration

Environmental parameters such as temperature have a correlation with component-level stress. As temperature increases, component chemical reactions and diffusion mechanisms are accelerated. This causes an acceleration or rapid aging beyond normal usage. This is beneficial for reliability testing, since test time is compressed.

The most widely used model for semiconductor failure rate acceleration is the Arrhenius model. This model is used to determine the semiconductor failure rate at a secondary temperature given an initial failure rate at an initial temperature.

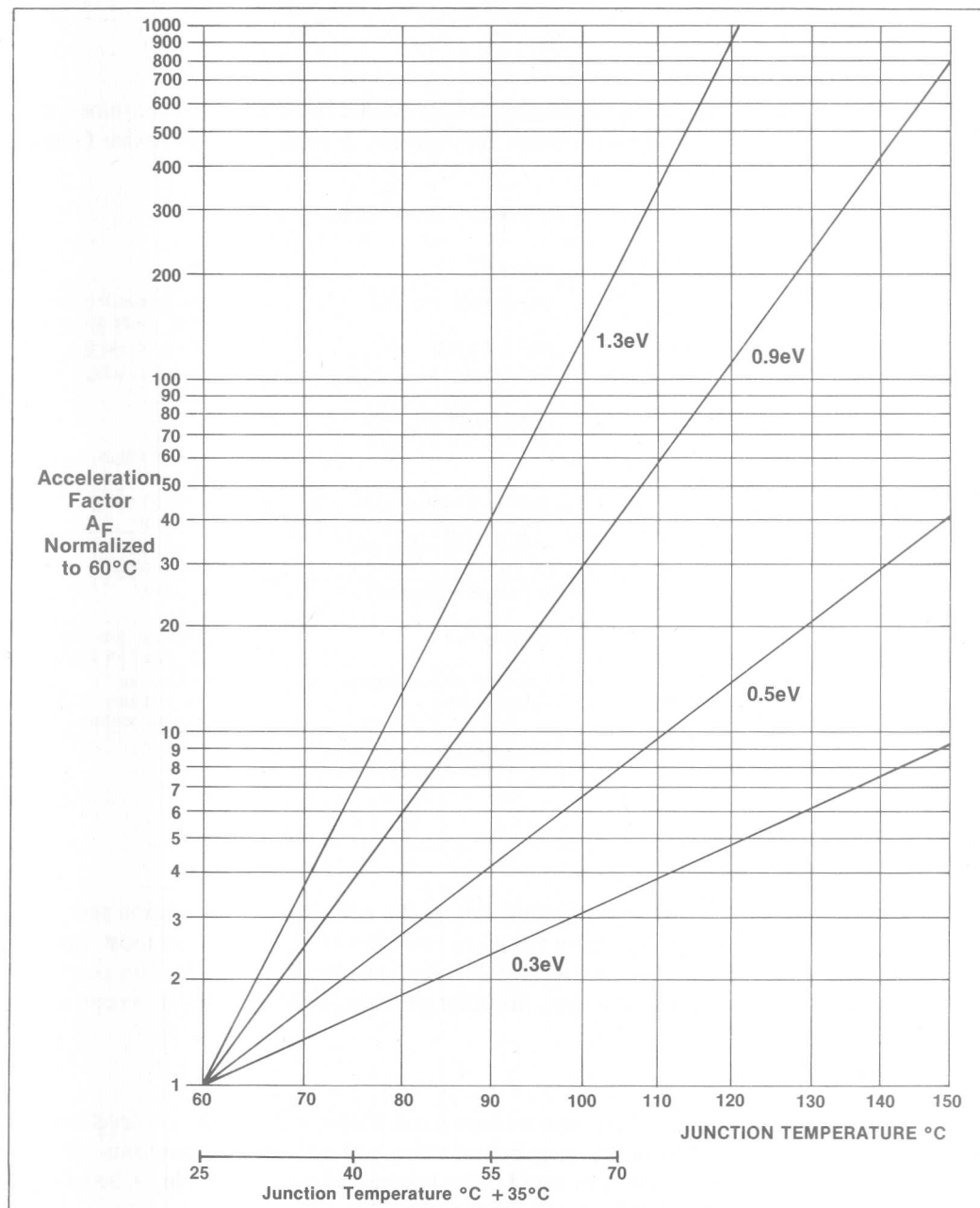


Figure 2-6. Arrhenius Acceleration Graph



Since activation energy is used in association with component reliability testing, the same method is applied to board and system acceleration. In accordance with a study of the MIL-HDBK 217E, a conservative activation energy of 0.5 eV is chosen for all acceleration calculations.

A typical usage of an acceleration factor is to translate accumulated unit test hours at an elevated temperature to the standard MTBF published temperature. For boards that are reliability tested at 70°C, unit hours are calculated for 55°C for board MTBF standardization.

example:

accumulated test unit hours at 70°C is 43,200 hours  
convert total test unit hours to 55°C

determine acceleration factor ( $A_F$ ) from Arrhenius plot  
solve by ratio on 0.5 eV curve

$$A_F (70^\circ\text{C} \rightarrow 55^\circ\text{C}) = A_F (70^\circ\text{C} \rightarrow 25^\circ\text{C}) / A_F (55^\circ\text{C} \rightarrow 25^\circ\text{C})$$

$$A_F (70^\circ\text{C} \rightarrow 55^\circ\text{C}) = 7.9/4.2 = 1.9$$

$$\text{test unit hours at } 55^\circ\text{C} = A_F \times \text{test unit hours at } 70^\circ\text{C}$$

$$\text{test unit hours at } 55^\circ\text{C} = 1.9 \times 43,200 \text{ hours} = \boxed{82,080 \text{ hours}}$$

### Demonstrated MTBF

Having completed failure analysis and determined the number of failures and total unit test hours, the point estimate MTBF and the demonstrated MTBF at the lower 60 percent confidence limit can be calculated. The point estimate MTBF is calculated as follows:

$$\text{point estimate mtbf} = \hat{m}$$

$$\hat{m} = \frac{\text{total unit hours}}{\text{number of chargeable failures}}$$

example:

total test hours = 82,080  
number of chargeable failures = 4

$$\hat{m} = \frac{82,080}{4}$$

$$\hat{m} = \boxed{20,520 \text{ hours}}$$

The in-house reliability demonstration test is based on a sample of units. To determine how representative the reliability test sample is of the population, we calculate the 60 percent confidence limit. In this manner we can state at a given confidence level that the MTBF of any unit from the population will be equal to or better than our demonstrated MTBF 60 percent confidence limit.

example:

A time-truncated test accumulates 82,080 hours with 4 chargeable failures at 55°C

$$\text{mtbf } 60\% \text{ lcl} = \frac{2T}{\chi^2(\alpha, 2r + 2)}$$

$T = 82,080$  hours = accumulated unit hours

$r = 4$  = number of chargeable failures

$2r + 2 = 10$  = degrees of freedom

$\alpha = .4 = 1 - (\text{confidence limit}/100\%)$

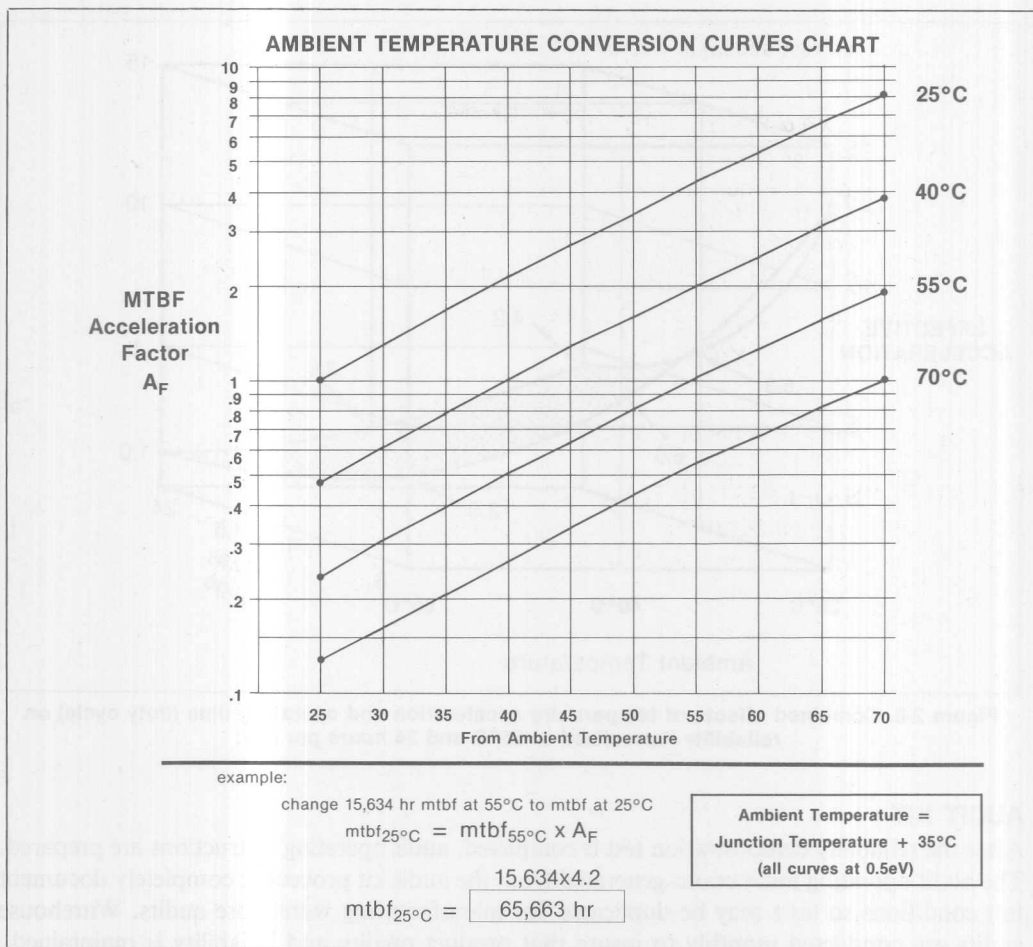
$\chi^2 = 10.5$  = chi-squared value at  $\alpha, 2r + 2$  (statistics table)

$$\text{mtbf}_{60\% \text{ lcl}} = \frac{2(82,080)}{\chi^2(.4, 10)} = \frac{164,160}{10.5} = \boxed{15,634 \text{ hours}}$$

The 60% lower confidence limit (lcl) states there is a 60% probability that the products true mtbf will equal or exceed 15,634 hours at 55°C.

### MTBF VERSUS OPERATING TEMPERATURE AND DUTY CYCLE

Although demonstrated MTBFs at 60 percent confidence are quoted at 55°C for boards and 40°C for systems, often lower temperature MTBFs (less stress hence higher MTBF) are requested. This is accomplished by using the previously established Arrhenius acceleration method.



**Figure 2-7. Ambient Temperature Conversion Curves**

For applications that do not require power 24 hours a day (continuous operation), an effective MTBF can be calculated using the cube model. The cube shown below illustrates the relationship of varying temperature and usage (average hours per day) and the effect on MTBF.

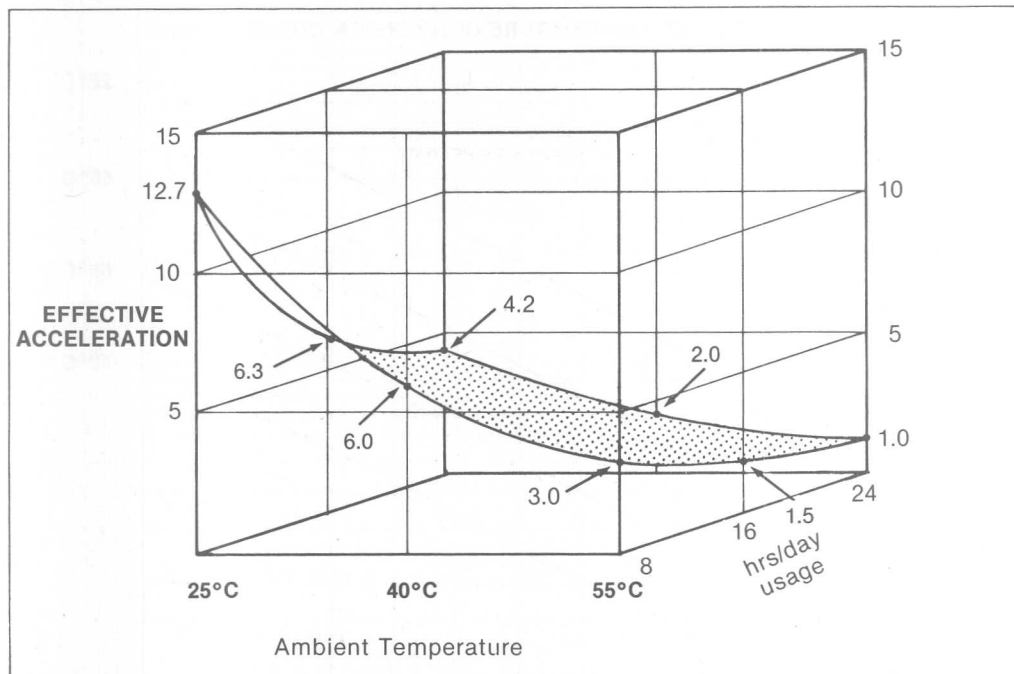


Figure 2-8. Combined effects of temperature acceleration and operating time (duty cycle) on reliability normalized to 55°C and 24 hours per day.

### AUDIT KIT

After the reliability demonstration test is completed, audit operating instructions are prepared. The audit operating instructions generated from the audit kit procedure completely document test conditions so tests may be duplicated for manufacturing warehouse audits. Warehouse audits are conducted monthly to insure that product quality and reliability is maintained.

### FIELD RELIABILITY

Field reliability data is periodically obtained from customers for reliability analysis. This is accomplished by working closely with customers to fully understand each customer's specific application, environment, duty cycle and failures. This information can then be compared against the MTBF prediction methodology and demonstrated in-house MTBF.

Field data on Intel products predominantly show a field demonstrated MTBF that is considerably larger than the in-house demonstrated MTBF. This is expected, since field data is based on a large population of units over an extended period of time as opposed to in-house demonstrated MTBFs that are based on small sample sizes and limited test time.

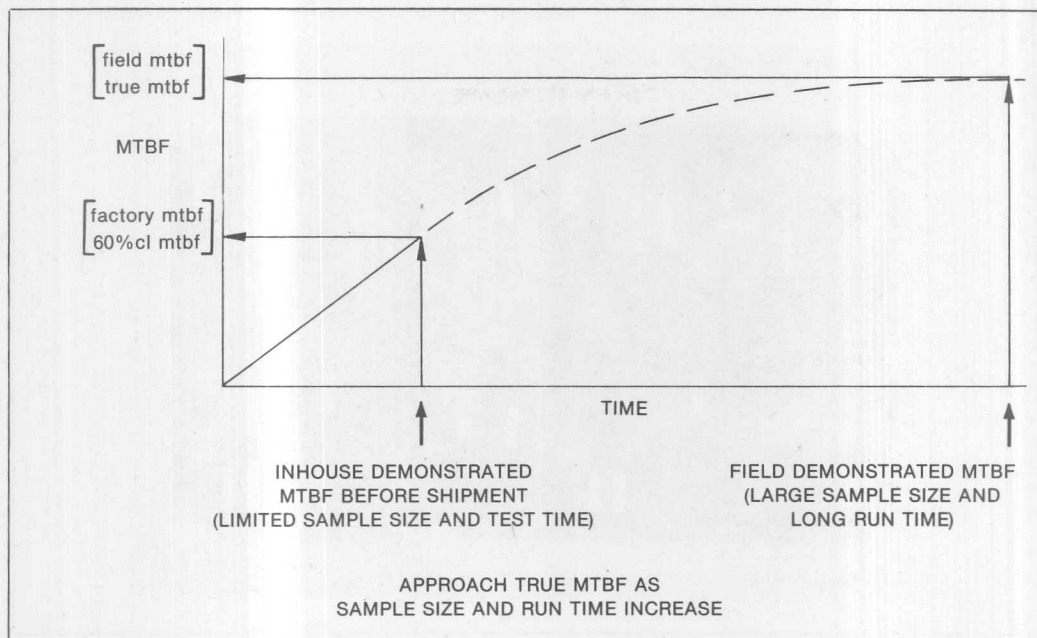


Figure 2-9. MTBF Limited Sample Size Versus Large Sample Size

### RELIABILITY DATABASE

Systems Reliability Engineering maintains a reliability database that contains information on board and system products. Typical database entries are MTBF predictions (at temperature) and in-house demonstrated MTBFs (60 percent confidence at temperature). The MTBF data is the most requested and is used for answering routine inquiries from our sales and marketing personnel in assisting our customers.

### RELIABILITY QUALIFICATION OF NEW TECHNOLOGY

New application technologies, such as surface-mount, require understanding and verification before implementation. Recently, surface mount technology (SMT) was incorporated into our product line to improve reliability and increase board functionality.

The Systems Reliability Engineering (SRE) organization worked closely with the design and manufacturing teams who were responsible for SMT process introduction. New product evaluation and test methods were developed specifically for SMT qualification by SRE. Considerable testing was performed in the areas of solderability, component placement, thermal stress and flex testing. These efforts have resulted in the introduction of new products that offer high reliability, high performance and increased functionality.

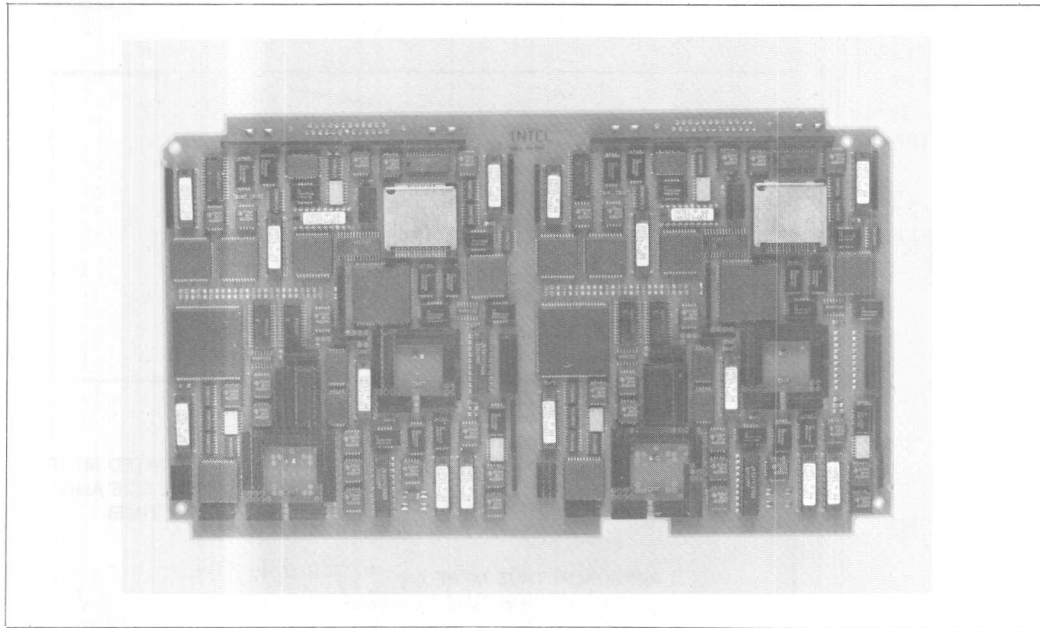
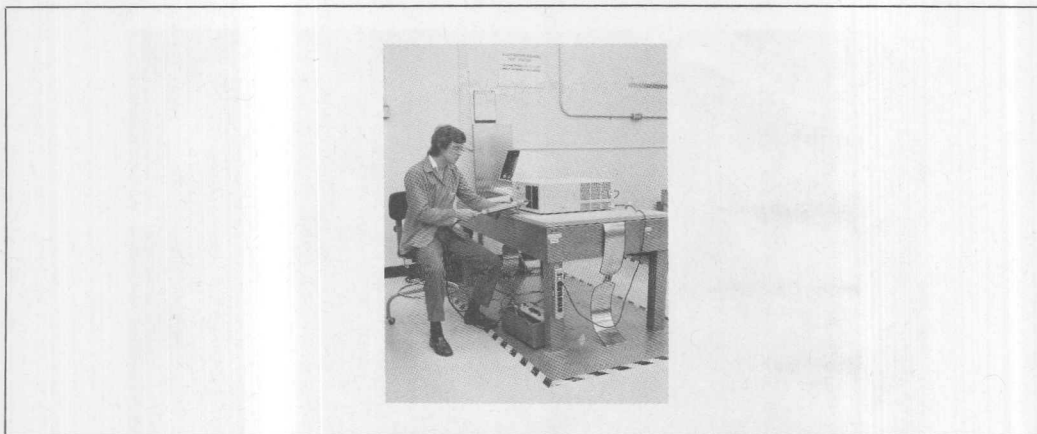


Figure 2-10. Surface Mount Technology

### ENVIRONMENTAL SPECIFICATION

The Systems Environmental Limits Specification defines the environmental requirements for all Intel board and system products. Both office grade and industrial grade environmental requirements are covered. In addition to the limits specification, there are test specifications that describe how specific environmental tests are to be performed. Standards and specifications used are:

- Electrostatic Discharge Standard
- Temperature Test Specification
- Humidity Test Specification
- Vibration/Shock Test Specification
- Altitude Test Specification
- AC Line Test Specification
- Acoustic Noise Test Specification



**Figure 2-11. Electrostatic Discharge Test Station**

### **ENVIRONMENTAL / RELIABILITY LABORATORY**

A centralized environmental/reliability laboratory supports all board and system engineering operations. The laboratory is used to perform environmental testing on all products during the qualification stage to insure environmental requirements are satisfied before product shipment.

Product design teams are free to use the facility for design evaluation testing as well as specification verification testing. In the event SRE is not able to perform a particular test, the laboratory staff will locate an available alternate lab.

The environmental/reliability laboratory is one of the most complete system house laboratories on the west coast. Inquiries are welcomed regarding usage of the test facilities.



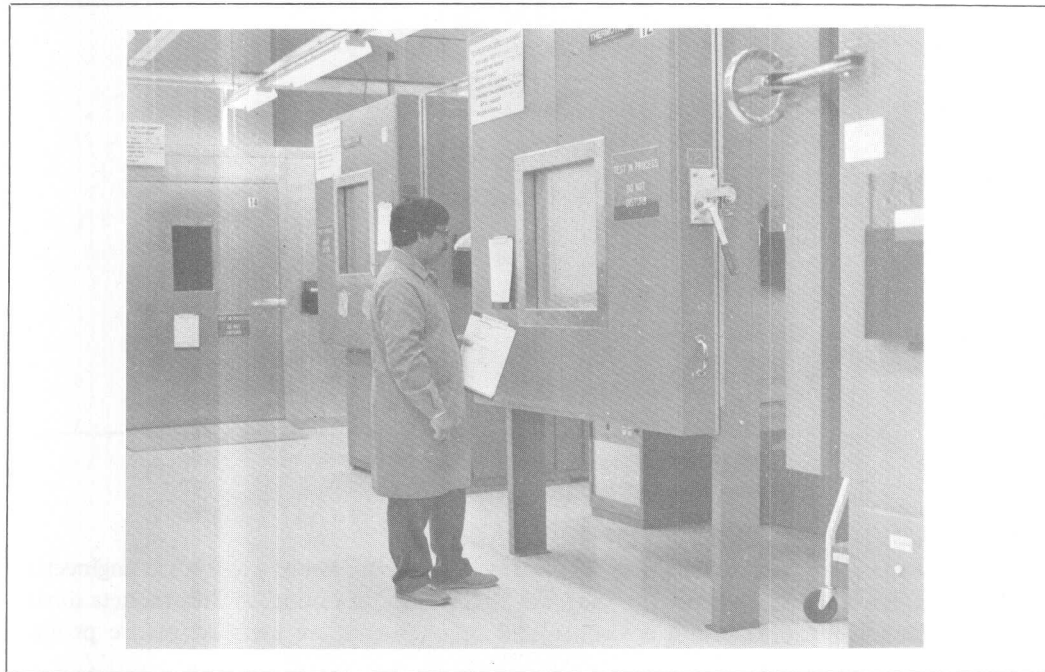


Figure 2-12. Environmental Laboratory

### Equipment

Intel has extensive environmental and reliability laboratories that include thermal scanning capability, vibration testing (sine and random), altitude testing, temperature testing, humidity testing, stress testing (quick temperature change), reliability testing, electromagnetic interference testing (EMI), electrostatic discharge testing (ESD), AC line testing and acoustical noise testing.

### Technical Administration

Each month a test forecast request sheet is sent to each engineering department for scheduling environmental and reliability testing over the next three months. The forecast sheets allow critical bookings, test schedules and maintenance issues to be handled smoothly.

Each request for testing is logged into a test log database. The database includes information on equipment used, tests run, test unit serial numbers and test results. The completed test log notebook is then archived for future reference.

The environmental/reliability lab reviews and makes recommendations based on the test data. Final decisions are made by the responsible engineering department involved.



Figure 2-13. Temperature/Low Humidity Walk-In Chamber

**Altitude Chamber**

64 cubic feet (4' x 4' x 4')/1.81 cubic meters (1.22m x 1.22m x 1.22m)  
altitude range: ambient to 100,000 feet (30,500 meters)  
limited temperature control to maintain safe operating temperatures.

**Thermal Scanner (thermal mapping)**

infra-red scanner—liquid N2 cools  
color monitor—12" (30cm) diagonal  
temperature range: 0 deg C to 200 deg C  
maximum resolution: 0.1 deg C per color step  
zoom capability to 16x

**Temperature/high-humidity Chamber**

64 cubic feet (4' x 4' x 4') 1.81 cubic meters (1.22m x 1.22m x 1.22m)  
programmable for temperature/humidity cycling  
temperature range: -73 deg C to +177 deg C (programmable)  
humidity range: 20% RH to 95% RH (programmable)  
temperature ramp rate: 2 deg C to 5 deg C per minute (programmable)  
laminar air flow

**Temperature/low-humidity Walk-in**

560 cubic feet (8' x 10' x 7') 16 cubic meters (2.4m x 3m x 2.1m)  
programmable for temperature/low-humidity cycling  
temperature range: -68 deg C to +85 deg C (programmable)  
humidity range: ambient to less than 10% RH (programmable)  
temperature ramp rate: 2 deg C to 5 deg C per minute (programmable)  
laminar air flow

**Temperature/stress chamber**

82 cubic feet (4.5' x 4.5' x 4') 2.3 cubic meters (1.4m x 1.4m x 1.2m)  
programmable for temperature cycling  
temperature range: -73 deg C to +177 deg C (programmable)  
temperature ramp rate: 2 deg C to 12 deg C per minute (programmable)  
dry air purge  
combined environmental test with shaker (future)

**AC Line Test Station**

line surge  
line frequency  
line voltage  
line drop-out  
inrush current

**EMI Shield Room**

EMI engineering investigation only  
radiated  
conducted

**Electro-static Discharge Test Station (ESD)**

voltage range: 0 v to 25 kv  
direct discharge  
indirect discharge

**Vibration Machine**

LDS model 824LS/DPA 24 shaker  
Spectral Dynamics model 1201 controller  
Kimball isolated step-base/slip-table  
gross machine weight: 19,000 lbs. (8,640 kg)  
maximum specimen weight: 1,000 lbs. (455 kg)  
maximum stroke: 2 inches (5 cm) peak to peak  
maximum force:  
sinusoidal: 6,000 lbs. (2,730 kg)  
random: 5,400 lbs. (2,455 kg)  
frequency range: 5 HZ to 2000 HZ

**Shock Machine**

MTS model 846.361  
MTS shock waveform analyzer  
GHI 16 channel shock wave form analyzer  
table weight: 500 lbs. (227 kg)  
maximum specimen weight: 1,3000 lbs. (590 kg)  
maximum acceleration: 600 g's

**Acoustic Noise**

Bruel & Kjaer model 2230 sound pressure meter  
Bruel & Kjaer model 4205 sound power source

Figure 2-14. Environmental Laboratory Equipment List

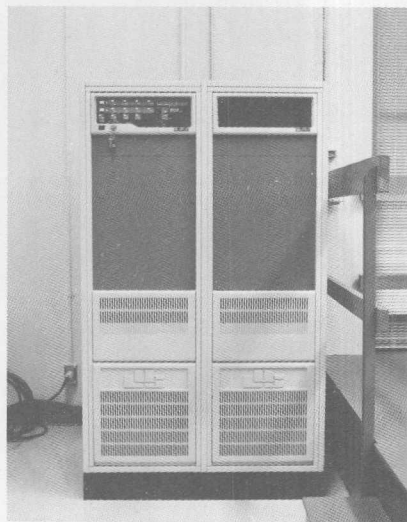
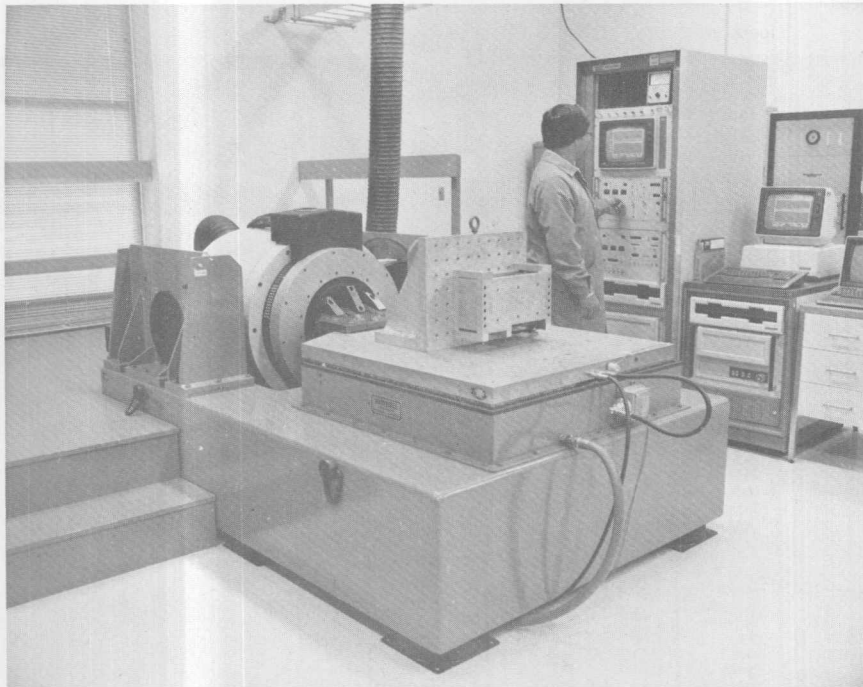


Figure 2-15. Dynamics Equipment



### Equipment Maintenance

All major lab equipment is on a routine preventative maintenance and calibration schedule. SRE maintain 100 percent conformance to calibration requirements every month. Each piece of equipment is checked for operational readiness before and after tests to assure that equipment deficiencies do not bias the test data or interrupt testing.

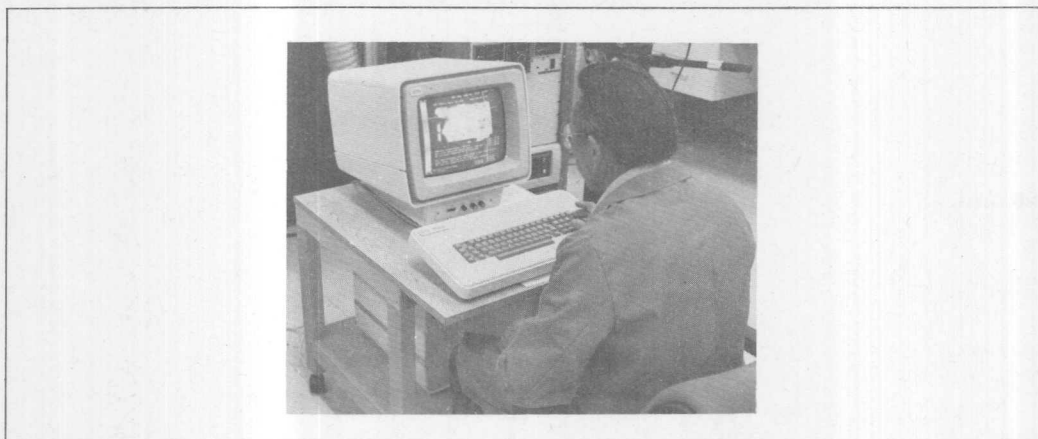


Figure 2-17. Thermal Scanner

### CONCLUSION

Intel Systems Reliability Engineering is chartered with providing the reliability program which guides the reliability effort during new product qualification. This is accomplished through policies and procedures, technical training and consultation, data collection and analysis, and directed research and development.

In support of product qualification, the systems environmental laboratory provides standards and specifications, a comprehensive environmental/reliability laboratory equipped for product testing/qualification, technical consultation, and training.

Systems Reliability Engineering at Intel is committed to delivering board and system products that offer the newest technologies and highest standards of reliability.









## **CHAPTER 3 MANUFACTURING**

### **A COMMITMENT TO WORLD CLASS MANUFACTURING**

Throughout Intel, a major emphasis has been placed on making our manufacturing capability equal to or greater than any company in the world. Systems Manufacturing has begun to reap dividends in terms of improved product quality and reliability. This chapter describes how our manufacturing processes contribute to building products at the highest quality level possible. We have focused on several areas:

- Implementing process controls throughout the factory
- Reducing our manufacturing costs
- Increasing our equipment utilization and productivity
- Increasing our process automation and data automation
- Developing our human resources through focused education and training programs

All of these efforts contribute to lower costs, higher quality and the reduced time-to-market our customers need to be competitive.

### **PRODUCT LINES AND TECHNOLOGY**

Intel manufactures a full complement of systems products, from printed circuit board products to computer systems at many levels of integration. We invented and have substantial experience in building single-board computers. Our expertise extends to memory expansion boards, microcontroller boards, communications boards, and both MULTIBUS® and Personal Computer form-factor configurations. We also design and manufacture custom form factors for boards up to 12" x 16" in size.

We manufacture a supermicrocomputer system family (SYP310/320) currently offered in a build-to-order range of configurations. Our system line also includes software development systems and a wide range of software products.

At Intel we intend to remain one of the pace-setting companies in circuit board technology, offering our customers maximum functionality in board and system products. In addition to our industry standard through-hole board technologies, we have state-of-the-art full surface mount capability.

Growing product functionality and density greatly increases the interconnect requirements of the substrate. Intel has responded to this challenge by developing multi-layered, fine line, and small via-hole printed circuit board (PCB) technologies. Intel's current complement of .062 inch-thick board technologies include multi-layer boards up to eight layers, fine lines down to .006 inch wide with .006 inch spaces, small vias down to .014 inch finished diameter and photoimageable soldermasks.

### Through-Hole Mount Track Density

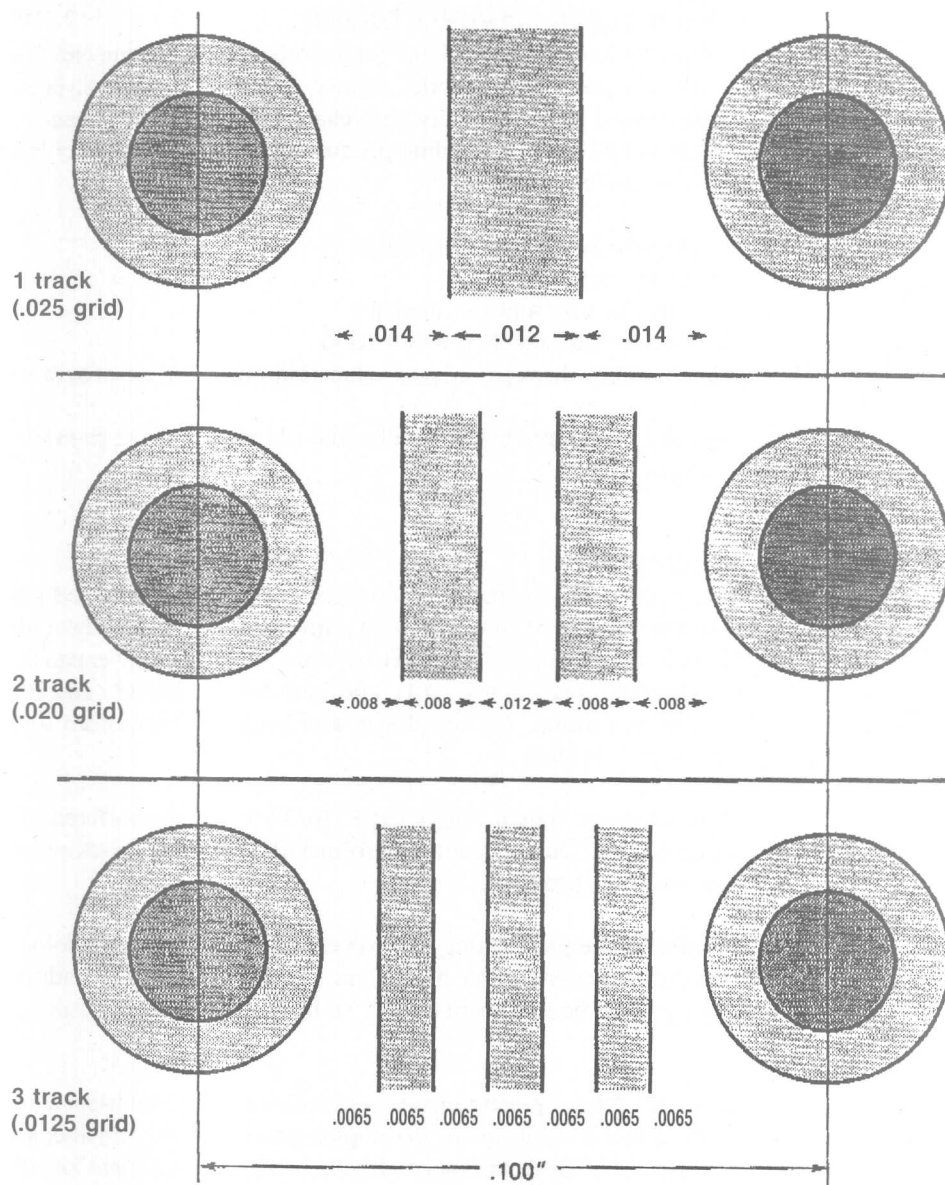


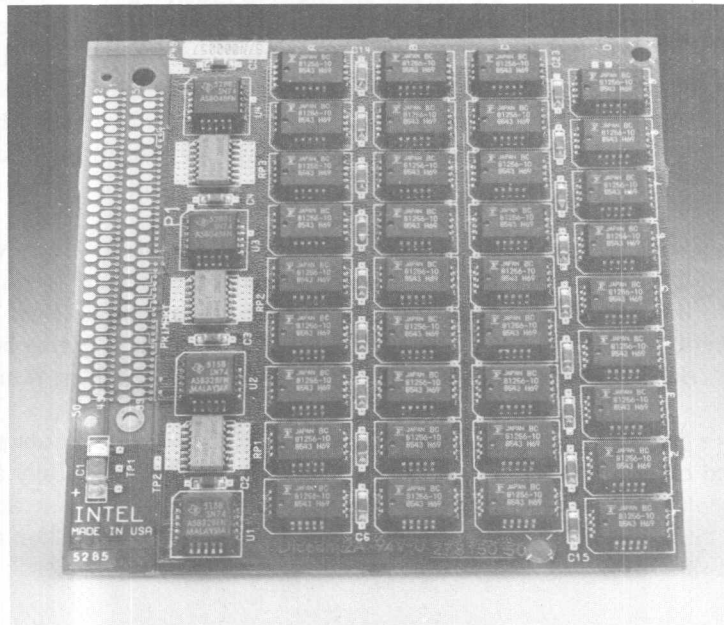
Figure 3-1. New Substrate Technology Results in Higher Track Densities and Thinner Trace Lines

Present methods of designing, assembling and testing conventional electronic assemblies using through-hole-mount technology, have reached their limits. Improvements in cost, weight, volume and reliability are hard to come by. Increased density, more functionality in a given enclosure or the same capability in a smaller enclosure combined with lower manufacturing costs are Intel's primary goals today. Surface Mount Technology (SMT) has helped to meet those goals. We have invested heavily in developing this capability for use on MULTIBUS® products.

SMT is a new packaging technology that replaces through-hole-mount components with surface-mount components. The assembly is soldered by IR reflow and/or wave soldering processes, depending on the mix of surface-mount and through-hole-mount components. The surface mount components, both actives and passives, when attached to printed wiring boards, form three major types of SMT assemblies, commonly referred to as Type I, Type II and Type III.

Type III SMT is a combination of through-hole components with surface-mount passive components mounted on the bottom of the circuit board. Type III SMT typically allows gains of 10 to 15 percent in real estate area, greatly improved electrical performance and increased reliability. Intel has an installed Type III capacity for placing over two million components per month (two-shift basis).

Type II SMT combines surface-mount and through-hole mount active and passive components on the top side of the board with SMT passives on the bottom side. It is a complex process involving both reflow and wave soldering techniques. Type II SMT typically produces real estate gains of 40 to 50 percent.



**Figure 3-2. Surface Mount Technology Yields More Functionality in Less Area**

Type I SMT is the full utilization of active and passive surface mount components placed on one or both sides of the board, eliminating conventional through-hole-mount components. Type I SMT requires reflow soldering exclusively and can provide up to 5X reduction in the size of an assembly.

Type I and II SMT processes are fully qualified and in production at Intel, with plans underway to develop a very high-volume surface-mount capability at an off-shore manufacturing facility. As product technology increases we intend to ensure that our manufacturing capability keeps pace with the quality and reliability requirements of our customers.

### **MANUFACTURING CAPABILITY**

To achieve maximum production flexibility and maintain high quality standards, Intel has developed focused factories that are optimized for specific manufacturing benefits.

We currently have three manufacturing sites, in Oregon, Puerto Rico and Singapore. All three have the same basic board manufacturing capability, with the exception of SMT assembly, which is installed in Oregon and Puerto Rico and scheduled for late 1988 in Singapore. Common processes across factories increases flexibility of manufacturing response and consistent product quality due to process consistency.

Though the same processes are employed everywhere, they have been optimized in different ways at the different sites to serve unique charters.

Our Oregon plant specializes in new product/process introductions, which are later transferred to our off-shore production plants. The Oregon site also provides a refinery service where final design and manufacturability issues can be worked out in a laboratory setting backed by a full complement of engineering services. In addition to a laboratory for very-quick-turn service, Oregon also serves as a manufacturing facility for low-volume and short life cycle products.

The Puerto Rico factory has been optimized to build stable products of many types and form factors with a quick throughput capability. The emphasis is on being able to mix multiple product line items of low to medium volume.

The Singapore facility is optimized for high-volume production with our quickest throughput capability. Singapore typically runs fewer product types but at higher volumes. As such, it can produce high quality products at very low cost.

Both Oregon and Puerto Rico sites manufacture systems as well as boards. The Oregon factory focuses on the introduction and production of high technology, low-volume product lines while the Puerto Rico plant uses state of the art automation to run higher volumes with quick throughput while maintaining build-to-order flexibility.

Manufacturing flexibility combined with process stability and consistency ensure the customer a quality product regardless of manufacturing location.

### **KEY STRATEGIES FOR MANUFACTURING QUALITY AND RELIABILITY**

Several strategies have been developed for enhancing our manufacturing performance. These are discussed in the sections that follow.

#### **Integrated Design, Marketing and Manufacturing**

We have established a quick-to-market product development methodology for linking product design, product refinement and production in one smooth process. Clear roles and responsibilities among the marketing, design and manufacturing players and cross-function teams help ensure swift execution of plans. Product manufacturability and testability are designed into Intel's products during early stages of product design with major manufacturing participation to ensure smooth transition into production. Quality and reliability issues are worked as an integral part of bringing new products to market.

#### **Design Rules**

Intel has developed a comprehensive set of product design rules and manufacturability guidelines to eliminate design-related manufacturing problems. Different criteria exist for systems and printed circuit boards. Each product type must adhere to a minimum subset of product performance criteria to qualify for production release and subsequent volume/low-cost manufacture.



**CAD/CAM Program**

Computer Aided Design (CAD) tools are used in all phases of design, from software to finished units. Today we are developing the first of several CAD/CAM (computer-aided manufacturing) links for software manufacturing. CAD/CAM links will shorten the product time-to-market cycle and provide real-time controls for both build-to-order and design-to-order methodologies.

**Procedures for Swift Execution to Production Release**

New product designs transition smoothly into manufacturing. This is due to manufacturing involvement in the product design/planning process from the very start. Each product has a cross-function team that manages the development and introduction process from design through the product's end-of-life phase-out. Through the use of project management tools such as design checklists, introduction procedures, formalized product training methods/content and management reviews, the project team is able to resolve potential problems before they become serious issues.

**Full-Service Refinery/Model Shop**

Intel has a full-service refinery/model shop to provide quick material acquisition and assembly and test capabilities in support of new products and processes. The refinery resolves remaining design and manufacturability issues, quickly preparing products for the manufacturing lines. Problems related to quality and reliability are identified and resolved through focused engineering effort before the product goes into manufacturing.

**CIM/CAM Program**

Another strategy emphasizes computer-based tools to improve manufacturing performance. We have established and are in the early phases of implementing a computer integrated business strategy that combines both computer integrated manufacturing (CIM) and computer aided manufacturing (CAM) technologies. The major features include real-time quality data tracking, automatic data input for work-in-process tracking, dynamic machine setup and real-time machine control. This program provides enhanced quality and process control, reduced manufacturing lead times and reduced inventory levels.

Our CIM/CAM program attempts to use Intel products wherever possible. Not only does this enhance our manufacturing capability, it also gives us important real-world experience with our products in typical customer applications. The knowledge gained as we work with our own products helps us understand how to improve their quality and reliability. Our PROM/PAL programming file server is an Intel System 310. Test failure data is collected on a System 310, and the wave solder process parameter monitor uses Intel's SBC® 344 and BIT-BUS™ boards. A 310 is also used in Puerto Rico to control the high-volume systems run-in module.

Table 3-1 shows some of the initial applications of CIM which use Intel equipment as controls or monitors.

Table 3-1. Intel Systems Products Add Value to Our Own Manufacturing Processes

Area	Product	Application
First Assy. Boards	SYP 310 iRMX® real-time operating system	The 310 PROM-PAL/Seiko File Server provides set-up information to the Data I/O programmers and Seiko robot. The system reduces machine operating time, cuts labor cost and improves programming quality.
Wave Solder Boards	RCB 4420 (Bit Bus)	Wave Solder Instrumentation provides real time monitoring of the operating parameters for the wave soldering and cleaning processes.
Test Boards	SYP 310	Barcode Pilot is part of the overall iFICS program. The Factory Information and Control System provides real-time information and control for the factory.
Test Systems	SYP 384 SYP 311	Integrated Manufacturing Monitor (IMM) Intel systems level products. It automatically loads test programs to each device for each configuration. This function provides Build To Order (BTO) testing capability.

## BOARD MANUFACTURING

Our goal is to design, implement and control manufacturing processes to enhance quality and reliability. The section below highlights aspects of our manufacturing process that add quality to the production process.

### Kitless Materials Strategy

For many products, incoming materials are delivered directly from receiving to manufacturing and stored at the point of consumption. This allows us to be "kitless"; i.e., raw materials never physically come together as a kit. Our goal is to reduce raw material handling, reduce warehouse space and lower inventory levels.

### PAL/PROM Device Programming Using Intel 310 System

For programming PROMS, PALS, and EPROM microcontrollers, we use Intel's System 310 as a PROM/PAL programming file server. The server provides set-up information to the Data I/O programming stations, reduces setup and operating time, cuts labor cost, and improves our programming quality. All masters of the PROMS/PALS are stored on hard disk and accessed through the System 310.

### Auto Insertion of Components

We use computer-controlled automatic insertion techniques to install over 90% of all dual in-line package (DIP) components; to sequence and insert axial components, stake pins and

jumper connectors (or plugs); and to apply solder mask. Universal Instruments Equipment is used to insert DIPs, axials and stake pins and is operated off the HOST program on Universal's software. A Seiko RT 3000 Robot inserts jumper plugs set up by the same 310 file server that drives data I/O PROM/PAL programming equipment. The robot is a standard piece of equipment with custom table and tooling designed by Intel.

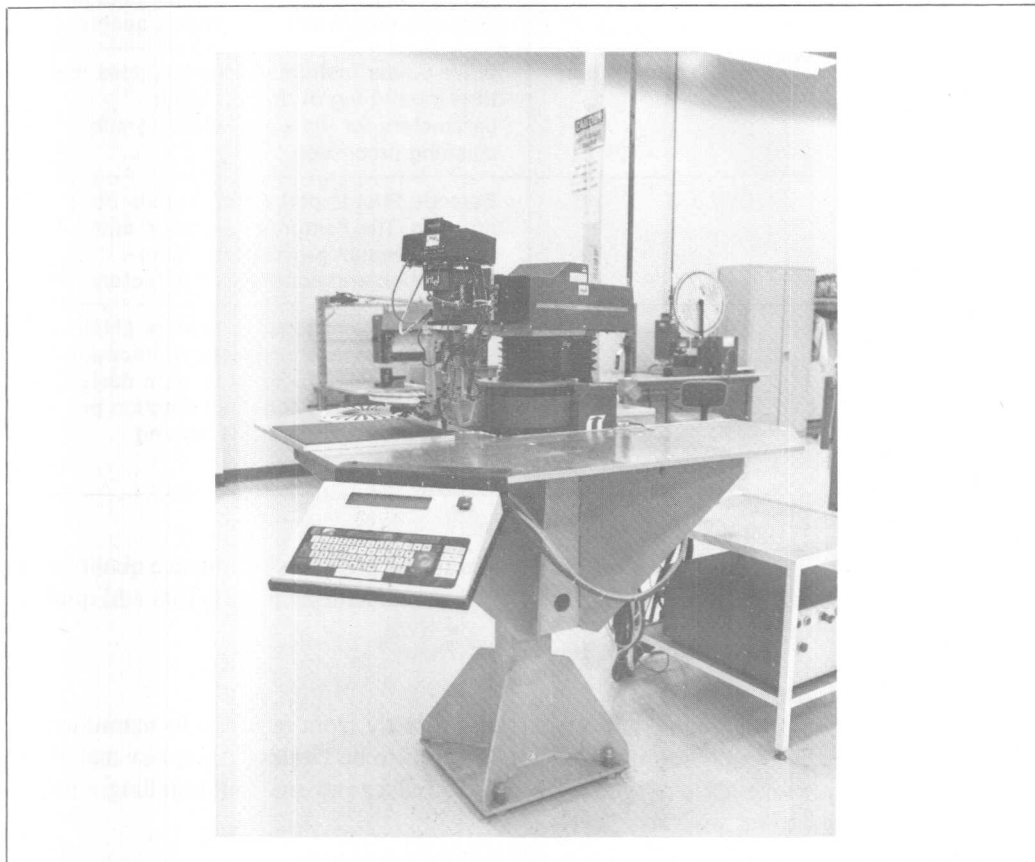


Figure 3-3. A Robot Inserts Jumper Plugs with a High Degree of Repeatability

#### **Surface Mount Technology**

We have full surface mount technology capabilities in both Oregon and Puerto Rico plants, with full capability for Singapore scheduled by Q3-88.

#### **Screen Printing**

For solder paste application for surface mount boards, Intel uses a Svecia screen printer. Instead of screens, we actually use .010"-thick stencils which have proven to give consistently high-quality prints. Stencils are produced from artwork. The artwork is created from the same CAD database used to design the circuit board.

Solder paste viscosity, a critical parameter, is measured several times a day with a Brookfield viscometer. Paste is stored under refrigeration and the shelf life expiration date posted on the container.

### Pick and Place (Primary Side)

Intel has installed Zevatech pick and place machines. Zevatech is noted for accuracy, repeatability and flexibility. The machine is capable of placing devices as small as 0805 capacitors and ICs with a footprint as large as 1.4" x 1."

Whenever possible, components are purchased in tape and reel for maximum component protection. Tape is specified as ESD-treated plastic. Passive components undergo an electrical test during the pick cycle. This test catches vendor errors and machine loading errors before assembly and soldering.

Zeva programming data is derived from the design database and is automatically converted and downloaded.

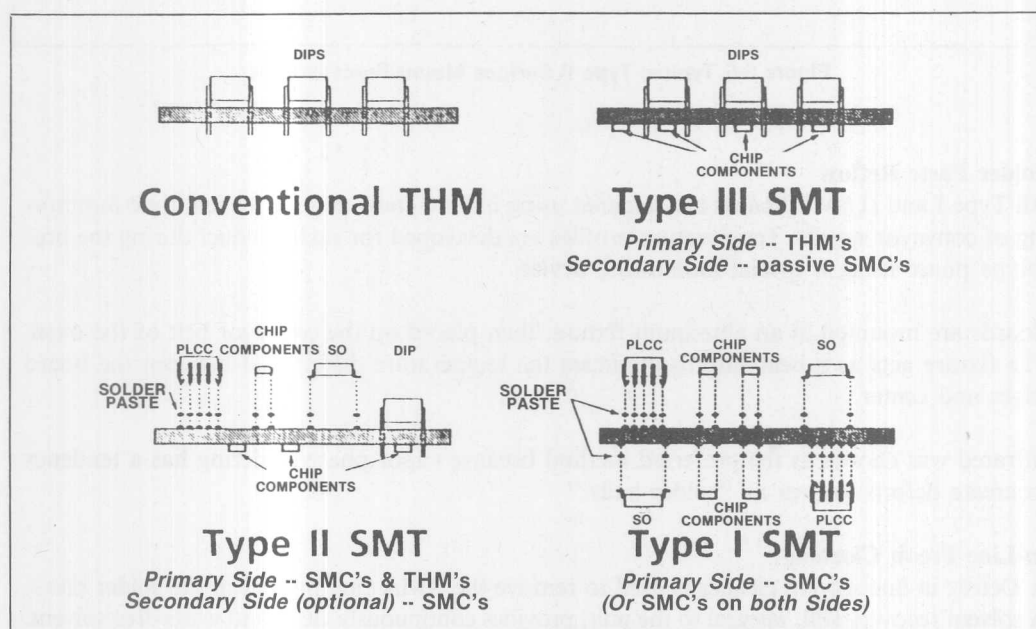


Figure 3-4. Comparison of through-Hole Mount (THM) and Surface-Mount (SMT) Component Placement

### Pick and Place (Secondary Side)

For Type III surface mount (chip resistors and capacitors), the board is turned upside down and sent through the Zevatech a second time. The first operation is adhesive application; a one-part thermally cured epoxy. The adhesive is purchased in 5cc syringes and stored under refrigeration to maximize shelf life. Lastly, the Zeva tests and places the passive devices.

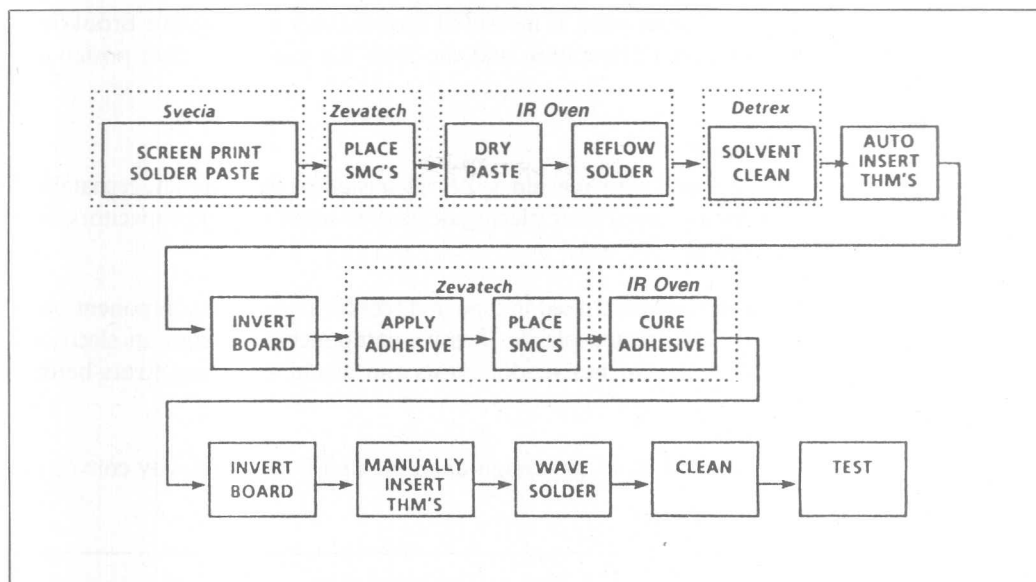


Figure 3-5. Typical Type II Surface Mount Process Flow

### Solder Paste Reflow

All Type I and II SMT boards are soldered using infrared heat zones with real-time monitoring of conveyor speeds. Temperature profiles are developed for each product during the prototype phase using a special monitoring device.

Boards are mounted in an aluminum fixture, then placed on the conveyor belt of the oven. The fixture acts as a heat sink to minimize the temperature differential between the board edges and center.

Infrared was chosen as the preferred method because vapor phase soldering has a tendency to create defects known as "solder balls."

### In-Line Freon Cleaning

A Detrex in-line solvent cleaner is used to remove the RMA flux present in the solder paste. A solvent recovery still, integral to the unit, provides continuously clean and water-free solvent.

### Adhesive Cure

Once again, the board passes through the IR oven. This time the temperature profile is considerably cooler for adhesive cure than solder reflow. This step cures the adhesive, holding the chip devices securely in place until wave soldering is completed.



**Figure 3-6. Zevatech Pick-and-Place Machine**

#### **Assembly Director Manual Insertion Technology**

Components that cannot be auto-inserted are manually inserted using a Royonics assembly director. The assembly director is a microprocessor-controlled system that uses a light beam to direct operators in placement of components on boards, while automatically presenting components at their workstations. Use of the assembly director reduces manual misplacement of parts by over 95 percent and improves productivity by 25 percent.

#### **Soldering Process**

Intel uses custom wave-solder fixtures of fixed external dimensions to eliminate wave solder machine setup. Assembled boards are loaded on a conveyor that carries the board over the solder waving machine and through an aqueous in-line cleaning system.

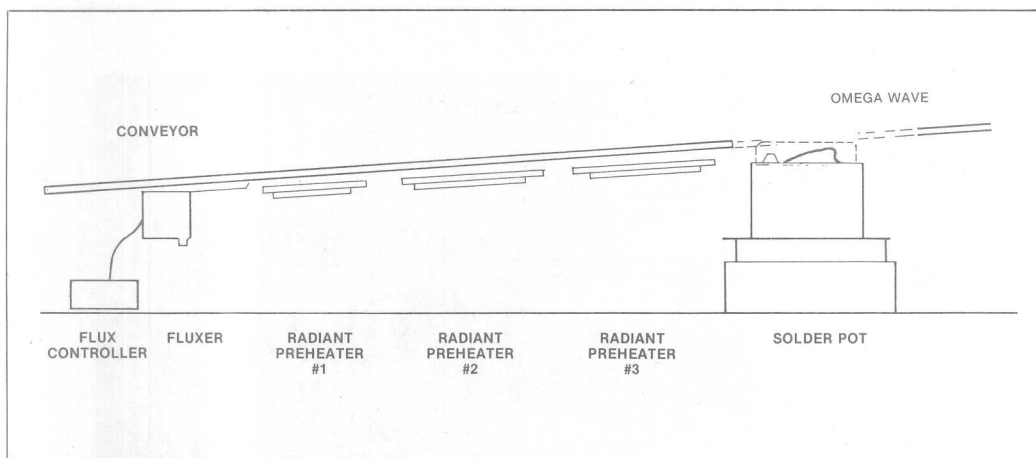


Figure 3-7. Wave Solder Machine (SMT Arrangement)

The wave solder process is monitored by our wave solder instrumentation system. Two Intel BITBUS™ boards (RCB 44/20s) monitor the desired parameters and transmits them to a microcomputer for processing. The wave solder instrumentation provides real-time monitoring of the operating parameters for the wave soldering and cleaning processes. A terminal beside the wave solder machine displays solder pot temperature, pre-heater and rinse water temperatures, conveyor speed and wash water flow rate pressure. We can also use auxiliary thermocouples to do temperature profiles of individual boards. Coupled with our statistical process control methods, we have driven solder defects to a very low level.

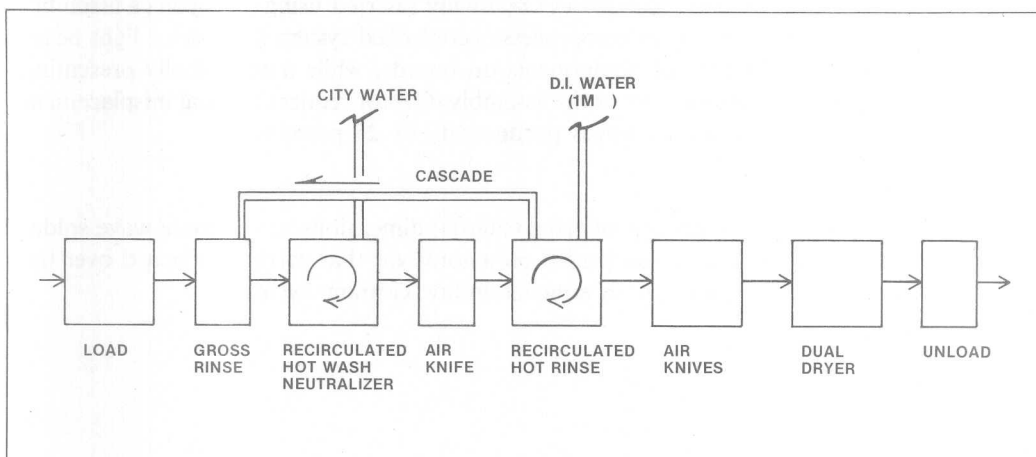


Figure 3-8. Aqueous Cleaner Schematic



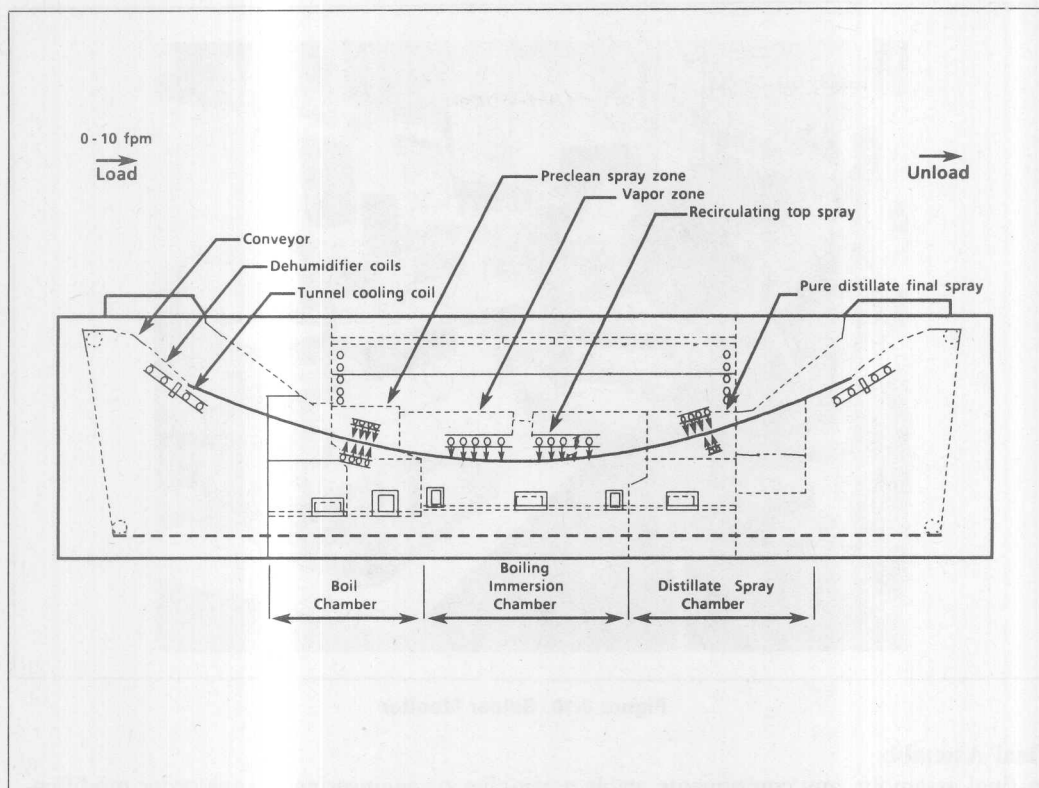


Figure 3-9. Detrex Solvent Cleaner



**Figure 3-10. Solder Monitor**

### **Final Assembly**

In final assembly, any components, cable assemblies or engineering change-order modifications that cannot be performed prior to wave solder are installed. Currently this assembly effort accounts for less than 10 percent of all component installation on boards. Operators in final assembly work to a solder/desolder process specification, which is designed to minimize pressure, time, and temperature of the solder iron on the board while ensuring a quality solder joint. All boards that pass through this area are cleaned in Dupont Freon TMS to remove contaminants.

### **Burn-in Reduction/Elimination Program**

Routine static burn-in at board level (SBBL) was discontinued in June, 1986 at Intel as a result of finding that less than .5% of all boards failed from burn-in-related causes. Discontinuing this process step reduced product cost and increased factory throughput for Intel and its customers. New product technology (e.g. surface mount) is still partially qualified with SBBL, which will continue until post-burn failure analysis indicates that a reliability goal has been reached.

During qualification, guardbanding of product specification is incorporated into SBBL to accelerate infant mortality. For example, a product specified to operate to a maximum of 55°C and voltages 12% of standard is guardbanded to 70°C and voltaged increased 6% ( $VCC = 5.3Vdc$ ). Static burn-in audits (with 100% die-level failure analysis) are guided by strict procedures to ensure that Intel process controls continue at high quality levels.

### Functional and STBL Testing

The test process starts in final assembly with the use of automatic test equipment (ATE). Boards are mounted on a bed-of-nails fixture for detection of any process-induced or material defects. Intel uses a variety of test vehicles to match required test coverage with board complexity. The Teradyne L200 family of testers is used to ensure the highest quality product possible for very high-speed, complex, function-rich boards. This machine, with its speed and large number of digital and analog channels, applies a stimulus to the unit under test through bed-of-nails fixturing, and evaluates the response providing guided-probe instructions to the operator for failure diagnoses. The test suite automatically administered to each unit provides a fixture continuity check, a product shorts and opens test, functional logic testing and in-circuit component test using software device modeling. Quality of product from this process step alone is expected to be 90 percent-plus failure-free; our goal by the end of 1988 is 97 percent-plus failure-free product. Where appropriate, Intel also uses GenRad 2272 testers for functional ATE test.



Figure 3-11. Teradyne L280 Test System

Once quality is at this level, the final test (STBL - system test at board level) is performed in a system environment using an edge-finger/backplane test fixture running at full product speed, with both voltage and temperature slew capability. The current (and always tightening) field quality goals for product subjected to this test process is always “guard-banded” so as to be equal to or better than our customers’ requirements.

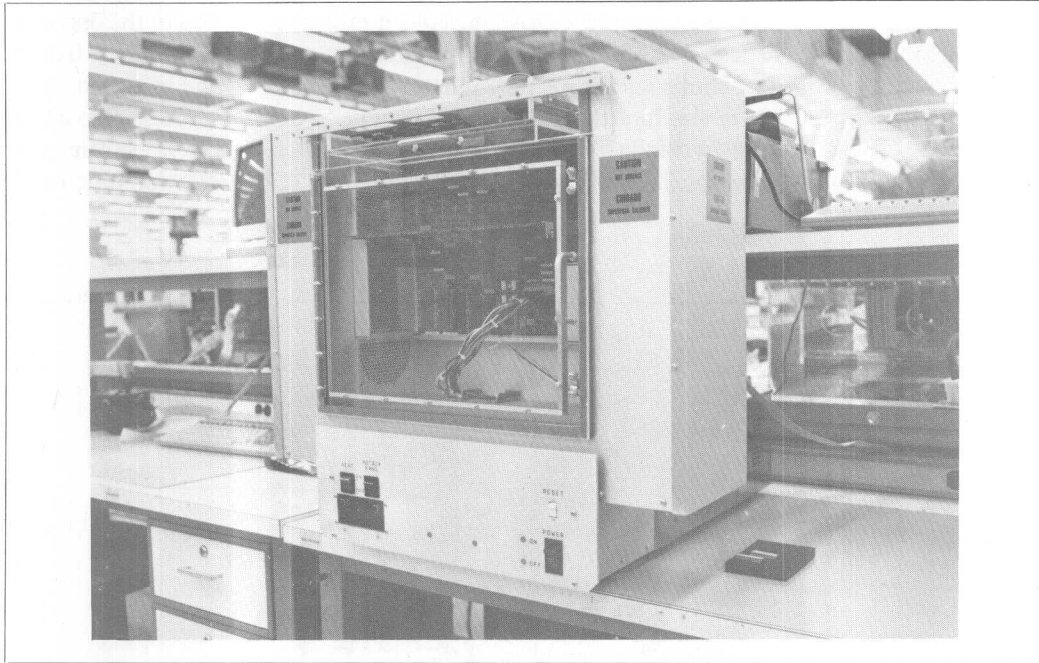


Figure 3-12. General Purpose Test Fixture

### SYSTEMS MANUFACTURING

As with board manufacturing, our systems facilities have concentrated on several process improvements to ensure a high level of manufacturing performance. The following highlights illustrate how our systems production capability contributes to high quality and reliability.

#### Automated Storage and Retrieval System (ASRS)

The Automated Storage and Retrieval System (ASRS) is Intel's multi-million dollar investment to improve our material handling and controls. The ASRS is a centralized raw material and finish goods warehouse located in our Puerto Rico production facility.

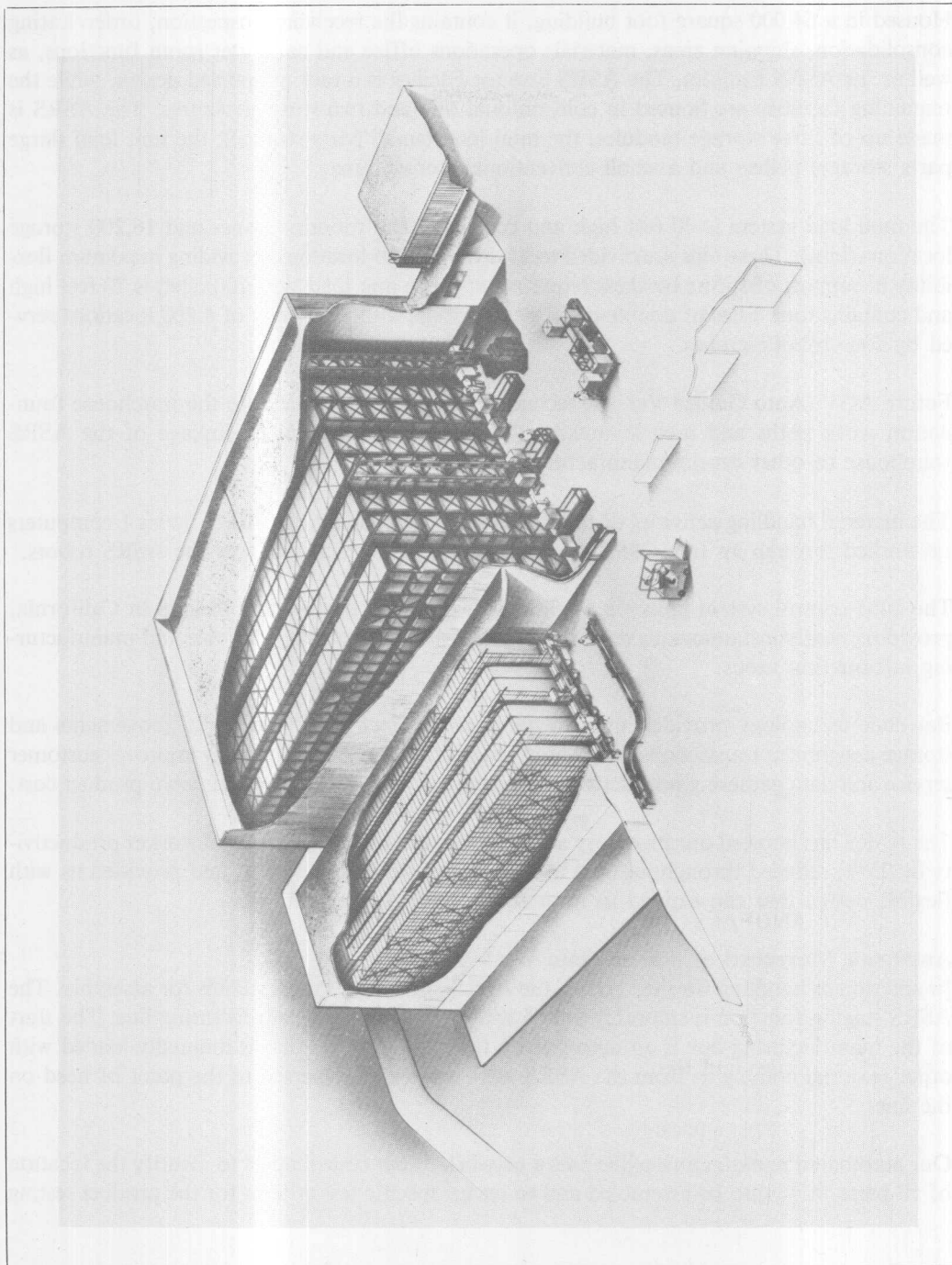


Figure 3-13. Intel Puerto Rico Automated Storage Retrieval System

Housed in a 64,000 square foot building, it contains the receiving, inspection, order/kitting consolidation, shipping areas, materials operations office and computer room functions, as well as the ASRS facilities. The ASRS Storage Facility is a rack-supported design, while the remaining facilities are housed in conventional one and two-story structures. The ASRS is made up of three storage modules, the mini load (small parts storage), the unit load (large parts storage) pallets and a small conventional storage area.

The mini load system is 40 feet high and contains three robotics cranes and 16,200 storage locations (bins). These bins are divided to 24 different sub-locations, providing maximum flexibility in support of future business requirements. The unit load system (pallet) is 70 feet high and contains four aisles of double-pallet-deep storage with a capacity of 4,800 locations served by four robotic cranes.

Future AGV (Auto Guided Vehicle) technology has been designed into the warehouse foundation work paths and area layouts that will allow the automated linkage of the ASRS warehouse to other on-site manufacturing facilities.

The material handling activities of the ASRS are controlled by two IBM\* Series 1 computers networked through an Intel 286-310 process controller which manages the ASRS robots.

The IBM control system links via satellite with our Intel host system located in California, providing nearly instantaneous response in supporting our customer service and manufacturing information needs.

Bar code technology provides input to the control system of our material movements and storage assignment transactions throughout the ASRS. Bar code technology improves customer service and data gathering productivity and accuracy, allowing us to hold down product cost.

The ASRS has boosted our inventory accuracy/control to 98%; improved worker productivity by 25%; reduced throughput time in system input/output by 50%; and provided us with flexible design that can expand to meet future business requirements.

#### **Automatic Movement of Material into Work Centers**

In addition to handling finished goods, the ASRS also stages raw materials for assembly. The ASRS staging function is smoothly linked with the automated manufacturing line. The start of the manufacturing line is an auto-gravity flow storage rack that is manually loaded with order material coming in from the ASRS warehouse and dispersed to the point of need on the line.

Our automated manufacturing line uses a network of bar code readers to identify the location of all parts waiting to be assembled and to set up specific test criteria for the product testing

\* IBM is a registered trademark of International Business Machines



process at the end of the manufacturing line. The products being built are assembled on hot pallets which flow from workstation to workstation until they are ready for test and burn-in.

At this point, a mini-load ASRS, which serves the dual purpose of testing and in-process storage, picks up the hot pallets and delivers them to a storage location, which is electronically set up for testing the specific product configuration for MTBF (mean time between failures) process controls. (The testing methodology is described below.)

After testing is complete, the products are packaged and labeled with a bar-coded product number and serial number before being shipped to the ASRS shipping warehouse.

#### **Build-To-Order (BTO) Flexible Production**

Build-To-Order (BTO) is a flexible structuring, forecasting and ordering process by which customers can select sets of functionality to configure an open system product solution specific to their needs. The BTO system determines the mix of products that move down the production line. All available options are forecasted and staged to support the final assembly process. Actual configurations are built only when a customer order is received. Since each order defines the specific final configuration, tests are created by the automated Integrated Manufacturing Monitor (see below) to test the quality of each configuration.

Advantages of Intel's BTO system include:

- The ability to configure the final system to a specific customer order.
- Minimal/no reconfiguration of systems and no shipment of aging warehouse inventory
- Factory throughput from receipt of order to shipment of two to three weeks
- The ability to accommodate unique small lot sizes in a high-volume production environment
- The final assembly schedule is limited to customer-specified configurations

#### **Integrated Manufacturing Monitor (IMM)**

Intel's systems are run-in tested using the Integrated Manufacturing Monitor (IMM), an Intel-designed system using Intel 310 Systems. It automatically assembles test programs for each system configuration, allowing us to "custom-test" our build-to-order products.

The IMM improves our manufacturing process by providing a shorter turnaround on test packages for new systems, simplifying the maintenance of test software, reducing operator intervention and reducing the paperwork associated with systems testing.

#### **SOFTWARE MANUFACTURING**

Intel has the ability to duplicate a wide variety of software media: 8", 5.25" and 3.5" diskettes are available in 33 different formats. The media is duplicated in an environmentally controlled room with temperature controlled to 70F +/- 5F and humidity controlled to 50% +/- 5% RH. This controlled environment allows precise duplication of media, assuring customers the ability to read their Intel diskette on any system.



All blank media are certified in lots using a diskette certifier that tests integrity and consistency. Diskettes are held for 24 hours in the controlled environment before programming to assure media stability. They're then duplicated on format duplicators. These machines are easily reprogrammed to duplicate new formats.



**Figure 3-14. Software Manufacturing**

In addition to the above diskette sizes, Intel has the ability to duplicate 1/4" data cartridges using an Intel SYP310-based duplication system. Intel also manufactures 1/2" magnetic tapes in several forms using VAX/MicroVAX\* equipment.

Intel software products are packaged on an assembly line to reduce material handling time and product cost and throughput time.

### **CONTROL SYSTEMS**

#### **Information Systems**

Intel has made substantial investments in developing state-of-the-art information systems. These systems support reductions in factory throughput, work-in-process materials and stores material, which, when combined with more real-time information, result in increased control and improved product quality.

\* VAX and MicroVAX are registered trademarks of Digital Equipment Corporation.

Systems are in place to support factory planning and scheduling, ensure that supplier selection is linked to the manufacturer approval process, and monitor material and manufacturing processes for compliance to quality requirements.

Major programs are underway to integrate more information systems, linking business and manufacturing planning, engineering design to manufacturing, and customer requirements to manufacturing capacity.

#### **Intel Materials/Manufacturing Automated Control System (iMACS)**

Intel Materials/Manufacturing Automated Control System (iMACS) is a semi-custom factory planning/scheduling system. It provides MRP-II planning technology by integrating our factory master schedules with our material planning and shop floor schedules to ensure we have both people and equipment available to meet customer demands.

iMACS enables Intel to start manufacturing activity on time and to complete the correct quantity at the correct time; to validate that materials are obtained only from approved sources; and to control the implementation of engineering changes using time-phased planning.

In 1987 iMACS was upgraded to provide additional on-line, real-time user interaction for updating schedules and executing orders. The business forecasting and customer order processing systems are also integrated into our factory system to enhance our ability to respond to customer requirements.

#### **Factory Information Control System (iFICS)**

The Intel Factory Information Control System (iFICS) increases our flexibility and responsiveness by providing extensive real-time, on-line shop floor status and control, on-line failure monitoring and evaluation for quality control, work-in-process tracking and control, and automated data collection. iFICS is also targeted for integration into our iMACS MRP-II and business systems.

iFICS will be used to monitor real-time wave solder processes; to reduce setup time through real-time loading of auto-insertion, robot and test instructions; to synchronize process instruction with product changes; and to initialize factory activity based on information obtained from the bar code identification label placed on the item. Currently, phase I of iFICS, involving automated tracking and monitoring of test failure data, is installed and operational.

iFICS reduces our costs, improves product quality, reduces our factory throughputs and enables us to provide customers with increased flexibility and responsiveness.

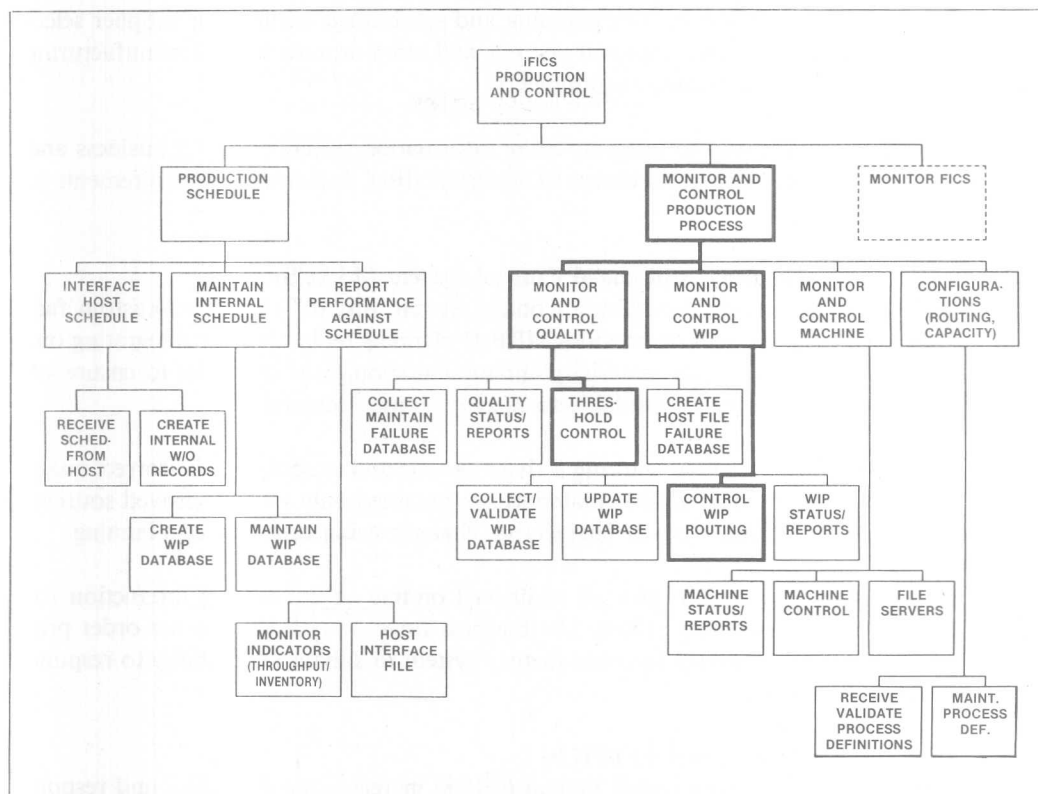


Figure 3-15. Intel Factory Information and Control Systems (iFICS) Provides Real-time Feedback

## MANUFACTURING SPC PROGRAM

Intel Systems Manufacturing began Statistical Process Control (SPC) implementation at its Singapore facility in mid-1985. Since that time, the program has expanded to include the Puerto Rico and Oregon facilities. Although the sites are geographically and culturally separated, their manufacturing SPC programs are standardized to ensure consistency and repeatability.

The Manufacturing SPC Program involves three key elements:

- Process control
- Product control
- Process-product optimization

### Process Control

Process control begins with identifying critical process parameters — those that contribute significantly to the overall process or product variation. Examples of critical process parameters in a manufacturing setting are wave solder temperature and conveyer speed.

Critical process parameters are first identified using SPC tools (such as cause-effect analysis, Pareto analysis, correlation analysis and designed experiments), then monitored and analyzed to pinpoint sources of out-of-spec variation. When all sources of variation have been eliminated or minimized for each critical parameter, the process is at a point of statistical control. Process control charts are then used to monitor process control.

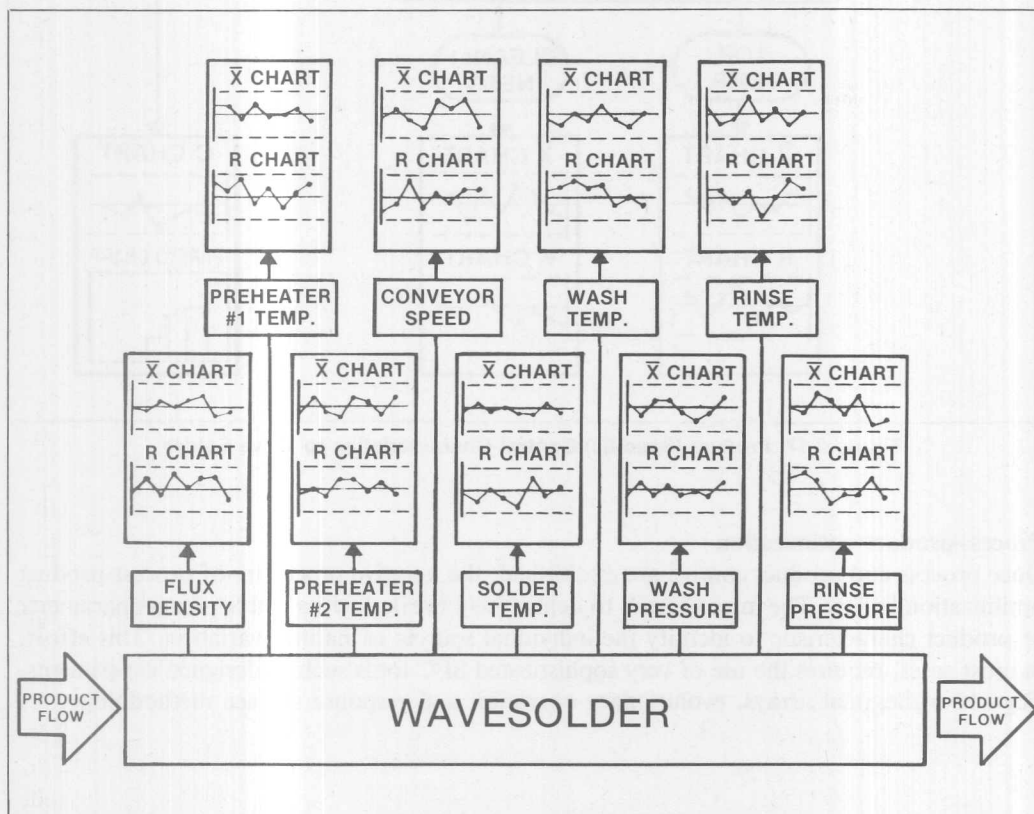


Figure 3-16. Process Control Parameters for Wave Solder.

### Product Control

Product control involves selecting critical product characteristics — those that affect the form, fit or function of the product — and eliminate errors in these critical characteristics through the use of SPC tools. Examples of critical product characteristics include solder defects and contamination levels. Product control checks not only previous parametric process controls but characterizes product-specific variations.

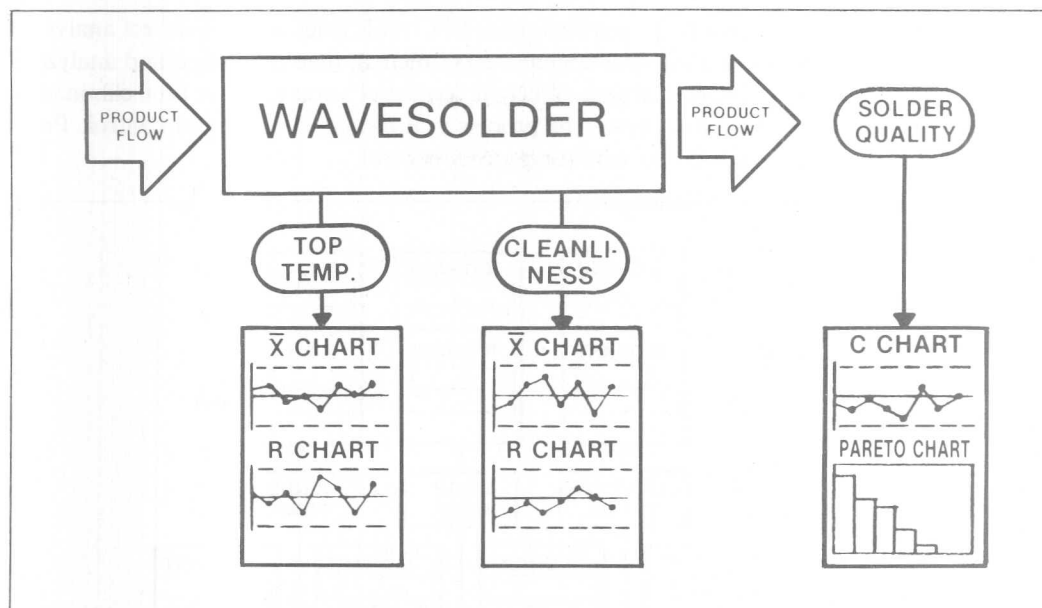


Figure 3-17. Product (Specific) Control Characteristics to Wave Solder

#### Process-product optimization

Once process and product control are established, the iterative procedure of process-product optimization begins. The intent here is to deliberately break down a stable process parameter or product characteristic to identify the individual sources of natural variation. This effort, in most cases, requires the use of very sophisticated SPC tools such as designed experiments, Taguchi orthogonal arrays, evolutionary operation and response surface methodology.

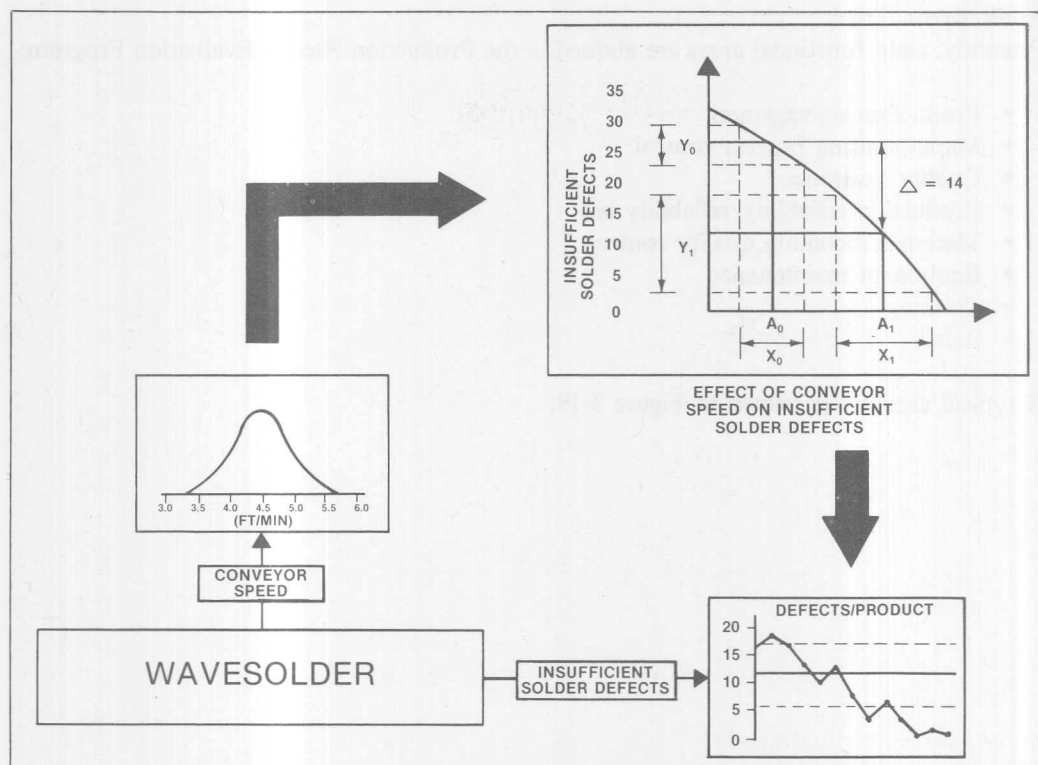


Figure 3-18. Example of a Typical Wave Solder Process-Product Optimization Experiment

Why experiment with stable processes? By continuously reducing the level of natural variation in the process parameters, the product resulting from that process becomes more consistent and predictable. The product-process optimization procedure, more than any other, illustrates Intel's commitment to continuously improve the quality and reliability of its products.

### PRODUCTION FACILITY EVALUATION PROGRAM

The Production Facility Evaluation Program (PFEP) is a factory audit program that ensures Intel production facilities meet or exceed all customer contractual requirements and Intel specifications. Initial evaluation occurs prior to start-up of any new facility and is repeated at least once a year to ensure continuous compliance. Production facility audits are conducted by senior Intel managers.

**Audit Areas**

Presently, eight functional areas are audited in the Production Facility Evaluation Program:

- Production management
- Manufacturing process control
- Quality assurance
- Production reliability/reliability lab
- Materials incoming quality control
- Equipment maintenance
- Training
- Safety

A typical checklist is shown in Figure 3-19.



NO. 187493 PRODUCTION FACILITY EVALUATION PROCEDURE Rev. 2 Page 6 of 22  
10.2

### MANUFACTURING PROCESS (GENERAL)

FACILITY \_\_\_\_\_ DATE \_\_\_\_\_ COMMENTS \_\_\_\_\_

ITEM		YES	NO	SCORE
1.*	Machine operating procedure exists for assembly equipment?			
2.	Daily equipment checklists in place and approved by M.E.?			
3.*	Equipment operators trained and qualified. Operators trained on use of MAI's. Operators certified to operate machine _____.			
4.*	Operator quality monitoring plan. Feedback to operator. Documentation available.			
5.*	Equipment PM/CAL data. Up-to-date. Listed on PM schedule.			
6.*	ESD requirements met. Wrist straps used. Mats grounded. Resistivity checks. Procedure followed. Procedure No. _____.			
7.	Hand tools available. Approved by M.E. Check for condition. Calibrated _____.			
8.*	MAI configuration controlled with respect to Engineering Documentation. MAI No. _____ Rev. _____, Eng. Drawing No. _____, Rev. _____.			
9.*	ECO change control process in place. Site interface established with SBS ECA. Regularly scheduled CCB meetings held. ECO dispositions comply with ECO Procedure No. _____.			
10.	P-site product transfer and product acceptance checklists comply with Rites of Passage Procedure No. _____, Rev. _____.			

#### \*CRITICAL ITEMS

This checklist will be supplemented by a specific checklist for the operational area as listed on IPP #145879, Q.A. Audit for Systems Manufacturing.

Figure 3-19. Typical PFEP Evaluation Checklist

Audits focus on three key elements: procedures, programs and process control.

**Procedural audits** verify that required procedures are at current revision levels and are, in fact, being used. Audited procedures include process documentation, product documentation, equipment calibration and maintenance, workmanship standards, production scheduling and control and material procurement. Workers must demonstrate a working proficiency in using procedures related to their areas.

**Program audits** verify that critical programs are in place and comply with customer and Intel requirements. Programs typically audited include quality control, training and safety.

**Process control audits** verify that all processes are controlled and are operating within customer and engineering specifications. Process control elements typically audited include the facility's SPC and electrostatic discharge (ESD) programs.

### **HUMAN RESOURCE DEVELOPMENT**

Intel Systems manufacturing has certification programs in place for all direct labor operators and assemblers in our factories. These programs are based on a workcenter curriculum that teaches the skills and quality standards required to execute one's job. The courses have been developed jointly by manufacturing engineering, quality assurance, production and operations training personnel and delivered by certified trainers. (See Figure 3-20.)



## TRAINING AND DEVELOPMENT PLAN

NAME \_\_\_\_\_ DATE OF HIRE \_\_\_\_\_

JOB TITLE \_\_\_\_\_ DEPARTMENT \_\_\_\_\_

MANAGER/SUPERVISOR \_\_\_\_\_

Use the Intel Training Catalog to assist you in filling out this plan.

I. **BUDDY** (if appropriate, assigned by supervisor)

II. **KEY CONTACTS** (matrix managers, SBS/Council chairpersons, support personnel, technical experts, trainers, etc.)

\_\_\_\_\_  
\_\_\_\_\_

### III. ORIENTATION

#### A. INTEL ORIENTATION

All new employees are required to attend orientation courses. At ITI employees will receive the list of appropriate orientation courses into which they will be automatically scheduled.

	Date Scheduled	Date Completed
Introduction to Intel (ITI)	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____

#### B. FUNCTION/OPERATION ORIENTATION (if available)

\_\_\_\_\_  
\_\_\_\_\_

### IV. CORE COURSES (teach skills/knowledge necessary for your job)

	Date Scheduled	Date Completed	Date Certified
_____	_____	_____	_____
_____	_____	_____	_____
_____	_____	_____	_____
_____	_____	_____	_____

Figure 3-20. Individual Training Plan

As with any manufacturing procedure, the course materials are catalogued, maintained and controlled through document centers to ensure their integrity and up-to-date status. Certification is based upon demonstrated performance at the end of training, with recertification required annually. These certification programs ensure that those working directly with product know the proper procedures and quality standards and the importance of their contribution to building high-quality product.

We also have a technical training and education program to keep employees current with changes in process and product technology. This is key to ensuring that Intel quickly assimilates new technologies while continuing to flawlessly execute current manufacturing plans. Training ranges from updates of the fundamentals (such as a printed board fab technology) to training on specific new components that will soon be introduced into manufacturing.

Ongoing technical education and training ensures that we maintain the state of our art and also allows us to quickly recognize and solve problems related to our manufacturing processes. We emphasize technical depth and problem-solving as important parts of our technical education programs.

In addition to in-house training, employees have access to important external programs such as the National Technological University, a satellite-based masters degree-focused university program conducted regularly at Intel domestic facilities.

Individual training and development plans help employees focus on their continuing education and development.

For Intel customers, our heavy emphasis on training contributes to our ability to produce high-quality products at low cost, due to our ability to understand our manufacturing processes and execute them crisply and cleanly.

## **CONCLUSION**

As a vendor of board and systems products, Intel aspires to world-class manufacturing status. Our philosophy of total quality, our many process control improvement programs, our focused efforts to educate our human resources and our reduction of manufacturing costs all combine to provide the quality, reliability and value that our customers expect.





## **CHAPTER 4**

### **PRODUCT REGULATIONS**

Intel recognizes its obligation to make sure its products do not cause injury or health hazard to the persons using and maintaining them. Intel is also committed to being an asset to any region in which it does business. Making its products comply with regional regulations and industry standards is one way to illustrate that commitment. For these reasons, Intel has established a comprehensive product safety and regulations program.

#### **RELIANCE ON EXTERNAL STANDARDS**

Intel is affected, directly or indirectly, by several independent international standards activities such as the International Electrotechnical Commission, the International Organization for Standardization, and the European Computer Manufacturers' Association. We play an active role in the Computer and Business Equipment Manufacturers Association (CBEMA), Underwriters Laboratories, Inc. (UL), and the Canadian Standards Association (CSA). We participate in CBEMA's Product Safety Committee for Data Processing Equipment; UL's Industry Advisory Conference for UL478, the standard used to evaluate the safety of most computer products manufactured and sold in the United States; and the CSA Subcommittee for Electronic Data Processing Equipment, the body that writes the Canadian safety standard for computer products.

Participation in the standards-making process is important to Intel for several reasons. It gives us a better understanding of the regulations themselves; it produces better communication between Intel and the product safety community; and it allows us to represent our unique product line in decisions affecting their sale and operation.

External standards are most helpful in describing regional idiosyncracies, in providing the latest consensus thinking on safety topics, and in keeping up with research on safety issues. However, Intel is cautious not to rely on external standards alone. External standards cannot adequately keep pace with the latest technologies such as surface mounting of components onto printed circuit boards and the newest methods of interfacing to computer equipment or telecommunications networks. Also, external standards do not always cover the unique features of Intel's products, processes and markets. Accordingly, Intel continuously develops its own safety requirements that go above and beyond the external standards.

#### **PRODUCT SAFETY COUNCIL**

At Intel, product safety activities are tied together in a cohesive, coordinated fashion and supervised by a carefully selected team of senior managers called the Product Safety Council.



The Product Safety Council (PSC) is an inter divisional body comprised of senior-level managers from Systems Manufacturing, Engineering, Quality Assurance, Risk Management, Legal, Customer Service and Product Safety. The PSC's charter is to review Intel practices and policies to make sure that any policy, procedure, practice or organization necessary to support the product safety program is in place and operating. Examples of the PSC's agenda include monitoring traceability and record retention and proceduralizing Intel's response to reported product safety problems.

## **PREVENTION**

At Intel, safety begins with prevention. Preventive activities include design support, audits of both products and processes, and response to reported safety problems.

### **Design Support**

To make sure product safety concerns are given top consideration throughout the design process, an Intel Product Safety Engineer (PSE) is included on every design team. This individual has signature authority at each stage of a new product's development, beginning with initial development plans and extending to the design phase releases, changes to engineering drawings and specifications, and even changes to Intel's Approved Manufacturers List, which specifies the suppliers Intel uses.

Intel has developed test specifications and design and program checklists that measure a product's conformance to stated safety regulations at each stage of its development. These cover all internal (Intel) requirements and external regulations (such as UL's), including the processes by which the new product is developed.

For example, while still in the planning process, the design team produces a document called the External Product Specification (EPS), a detailed description of the product's attributes measurable by the user. The EPS defines the interfaces between the product and its environment, including electrical, mechanical, reliability, software and operator interfaces. The Product Safety Engineer participates in creating this document, specifying which regulations must be met and which certifications obtained.

After prototypes are built, the Product Safety Engineer conducts a first-pass product safety evaluation to check compliance to applicable regulations. Any problem areas are identified and resolved before product development proceeds.

During the next phase of product development the Product Safety Engineer assists in writing the Qualification Plan. This document details the functional evaluation, product safety, environmental and reliability tests to be used in qualifying the new product. The plan must include an evaluation against a detailed design safety checklist and product safety test specification (see Figures 4-1 and 4-2).

**PRIMARY CIRCUIT COMPONENTS AND USAGE**

- Power Cords and Their Connections
- Strain Relief
- AC Wall Plugs and Power Outlets
- Air Gap Devices (Switches, Relays, Breakers, Contactors)
- EMI Filters
- Transformers
- Fans and Motors
- Fuseholders and Fuses
- Internal Wiring
- Terminal Blocks and Connectors in Hazardous Circuits
- Optical Isolators and Solid State Relays
- Labels
- Purchased Electrical Assemblies (Power Supplies, Floppy Disk Drives, CRT Assemblies, etc.)

**ELECTRICAL REQUIREMENTS**

- Overcurrent Protection
- External Interconnecting Cables
- Battery Back-up

**MECHANICAL REQUIREMENTS**

- Grounding and Corrosion Protection
- Accessibility
- Interlocks
- Enclosures
- Flammability
- Terminals for Field Wiring
- Markings
- Manuals
- Disposal Considerations
- Conductive Coatings

**TESTS****ERGONOMIC CONSIDERATIONS**

- Display Units
- Keyboards
- Controls & Lights

**Figure 4-1. Design Checklist**

A design release meeting is held before the product is released to manufacturing, with the Product Safety Engineer again participating. During this meeting process, the design release checklist must be completed, along with a signed design release product transfer form. All required product certifications must be completed before the product can be release to production.

**Auditing**

To make sure product safety and regulations activities are fully integrated into the company and everyone understands their role with respect to prevention, Intel conducts periodic audits of both the products and the processes Intel uses to run its business.

Product audits are product-specific audits supervised by the Product Safety Auditor (PSA) for each manufacturing site. The PSA is selected by the quality manager of that site and is responsible for product safety compliance at that factory.

**ELECTRICAL PRODUCT EVALUATION TESTS**

- Conditions for Test
- Test Equipment
- Input Current
- Earth Leakage Current
- Temperature Rise
- Ground Continuity
- Dielectric Voltage Withstand Test
- Stored Charge Test
- Abnormal Tests

**PRODUCTION TEST**

- Conditions for Test
- Test Equipment
- Ground Continuity Test
- Dielectric Voltage-Withstand Test (HIPOT)

**PHYSICAL STABILITY**

- 10 Degree Tilt
- Lean
- Foothold

**MECHANICAL STRENGTH FOR ENCLOSURE**

- Deflection Test
- Impact Test
- Strain Relief Test

**FLAMMABILITY TESTS**

- Thermal Aging Test
- Flammability Test
- Extreme Temperature Test
- Hot-Wire Ignition Test
- High-Current-Arc Ignition Test

**REPORTING OF TEST RESULTS**

- Applicability
- Records Retention
- Test Record Content

**Figure 4-2. Product Safety Test Specification**

Product audits include the auditing of incoming materials to make sure they comply with Intel's specifications and the inspection procedures written by or for external regulatory organizations.

Product audits are extensive, checking for things such as the distances between electrical parts, proper grounding, presence of warning labels, wire routing, insulation integrity and proper vendor of parts. Any discrepancies between the product and the regulatory organization's inspection procedures are reported to the Product Safety Engineer, who is responsible for resolving the discrepancies. The Product Safety Auditor monitors resolution of any problems found.

Process audits are the backbone of Intel's product safety program and encompass engineering, marketing, sales, repair, manufacturing, quality control, materials, reliability and calibration procedures.

The product safety audit focuses on global, non-product-specific topics such as record-keeping; traceability; design and manuals control; manufacturing control; follow-up and corrective action; testing; written policies, procedures and instructions; field reporting procedures; customer awareness; repair control; recall readiness; supplier control and quality control.

Intel's product safety audit philosophy extends to its suppliers. We have developed individual product safety and regulations criteria tailored to each commodity category, from power supplies to plastics.

### **Response Capability**

A significant part of preventing product hazards is responding rapidly to reported product safety problems, whether they come from the production line or the field. For this reason, Intel has developed a standard written procedure that outlines the steps required to initiate a response to a problem. The procedure specifies the people that must be notified, the type of background information that must be obtained, and the individuals responsible for response. A follow-up report is required to make sure the response was fast enough, to assess the cost of fixing the problem versus the cost of preventing the problem, and to make sure records of the problem are thorough and properly archived.

If a safety hazard is discovered in a product already in the field, a separate, special-purpose procedure comes into play. The procedure describes the various levels of response to such situations, including everything from a letter to the customer to immediate repair at the customer's site. It describes a number of detailed methodologies appropriate for various types of problems and assigns appropriate levels of reporting and decision-making.

## **CERTIFICATION**

### **The Regulations Environment**

Product regulations are imposed for a variety of reasons, such as to protect the public against unreasonable risks of injury or loss, to prevent unreasonable interference with radio and TV communication, and to make sure that products connected to public telecommunications networks will not introduce problems when connected. These regulations are developed, introduced and enforced by a number of organizations, ranging from private industry groups to government groups at local, regional, federal and international levels.

Computer products typically are certified by several independent safety certification organizations. Most major U.S. cities require all computer products sold or used within the city limits to be certified by an independent third-party organization such as UL. In Canada, computer products that are sold, used or displayed are required, by Canadian Provincial laws, to be certified by the Canadian Standards Association.

As governments become more sophisticated and concerned about computer usage, the number of regulations increases. Regulation complexity, too, is increasing. For example, custom plastic parts used in UL Listed products must now be purchased only from approved molders and fabricators that are audited periodically by UL.

Regulations also change constantly, due to efforts towards international coordination, changes in technology and ongoing research into safety topics.

Intel's Product Safety Engineers are responsible for keeping up with the changing regulations environment to ensure that Intel products are in compliance with or ahead of the latest thinking on product safety.

### **Electromagnetic Interference (EMI) Reduction**

Of significant concern to computer manufacturers today is the amount of electrical and magnetic interference (EMI) their products generate. EMI is caused by the very fast changes in electrical voltages and currents inherent in computer products and is emitted either through the air (radiated emissions) or through the power cord (conducted emissions). These emissions can interfere with communications, such as radio and television reception, sometimes in the form of "snow" or background buzz.

To control electromagnetic emissions in new product design, Intel trains design engineers in EMI reduction and conducts frequent EMI emissions measurements throughout the product development cycle.

### **Ergonomic regulations**

Another product regulations topic of concern to Intel is ergonomics, which is the study of product design factors that affect the ease with which humans operate machines. Ergonomic considerations include the product's noise level, the degree to which it causes eye or back strain, and overall ease of use.

Intel designs products in compliance with West Germany's ZH1/618, an ergonomics standard, which specifies such safety parameters as computer monitor contrast, resolution, reflectivity, tilt and height. Intel developed its own acoustic noise specifications.

### **Certification Strategy**

Intel's certification strategy — the process of determining which regulations and certifications are appropriate for a new product — is determined during the early phases of new product development. Intel considers several factors. One is the intended use of the product: Will it be sold into an OEM or end user market? Will it be used on a lab bench, in a computer room, an office or a home? Will the product be connected to telephone lines?

Another determining factor is Intel's view of the future of related product regulations. For example, it may be sufficient for older products to comply with the fourth edition of UL478 if Intel plans on phasing out the product before the fourth edition of UL478 becomes invalid. New products, on the other hand, would most likely be certified for compliance with the fifth edition.

Intel also considers market sensitivity to regulations compliance. Some countries are more sensitive to specific regulations than others. Some accept certification only from certain organizations. In West Germany, for example, proof of compliance to federal safety law can be obtained from the Verband Deutscher Elektrotechniker (VDE), Technischer Überwachungs-Verein (TUV) and several other German certification organizations. In the U.S., products in the highly technical end-user test equipment market are certified by ETL Laboratories or UL; products in categories such as OEM data processing equipment, however, require UL certification only. Table 4-1 shows the most commonly used regulations for data processing products by region.

**Table 4-1. Computer Safety Standards**

Region	Office Equipment	Computer Products	Combined Standard
US	UL114	UL478 4th Edition	UL478 5th Edition
Canada	CSA C22.2 No. 143	CSA C22.2 No. 154	CSA C22.2 No. 220
Germany	VDE 0806	VDE 0805	VDE 0805
British Commonwealth Countries	BSI 3861	BSI 6204	IEC 950
International	IEC 380	IEC 435	IEC 950

To keep pace with rapidly changing technology, Intel must obtain certification quickly. We also need to obtain fast UL/CSA evaluations of alternate component sources such as switches, filters, power supplies and peripheral assemblies, to keep manufacturing costs competitive. Intel does this by maintaining a close relationship with certification organizations and a current understanding of preferred certification procedures.

#### **TRACEABILITY**

To take fast remedial action in the event a significant problem is discovered in a shipped product, Intel makes it a policy to know the first point of sale for each product it distributes. We do this through a traceability system that tracks the identity and location of products and key subassemblies from Intel assembly lines to individual customer locations.

At the start of a new product's development cycle, members of the design team come together to select those items in the product that represent the most significant safety and quality risks. Those items are designated Controlled Items. Controlled Items are marked with serial numbers or date codes that are recorded during the manufacturing process. These records are used to trace faulty parts or products back to their point of origin. Intel focuses on knowing which Intel product each controlled item is in, on knowing that product's serial number, and on tracing the manufacturing process by which the product was produced. We're then able to match these identification records with the names of customers who purchased the products in order to notify them if a problem occurs.

Our traceability objectives consists of the following elements:

- Process records kept at the point of manufacture of an item or group of items
- Distinctive marks (lot codes, date codes or serial numbers) applied to each item at the point of manufacture
- Configuration records of the particular Systems product in which an item is ultimately installed and shipped
- Shipment records, by part identification and lot, date or serial number, to the first point of sale
- Maintenance transaction records on controlled items removed and replaced as a result of maintenance or field changes

A good record-keeping system is essential to a prompt, efficient traceability program. For this reason, Intel archives exhaustive data on all parts and manufacturing processes. We save all test data sheets and records, design team meeting minutes, correspondence involving product safety matters, and production and sales traceability records. These records are kept on file five years after a product has been phased out.

Product safety records are archived in record retention centers. Formal record retention centers are housed in buildings specially protected against natural disasters (such as earthquakes), environmentally controlled with respect to temperature and humidity, and under maximum security to protect from vandalism and industrial espionage.

All records retention activities are governed by explicit records management policies and procedures.

### **SAFETY TRAINING**

Intel recognizes that its performance and success are determined by its ability to develop the talents and skills of its employees. That's why we have developed an extensive employee training program, called the Intel University, geared to training employees in the standards, processes and procedures that Intel uses.



Because we believe that product safety begins with individual employees, we have a training program tailored to product safety activities. These courses are directed at project managers, design engineers, QA inspectors, assembly line workers and field repair personnel. Our product safety courses provide the foundation on which Intel safety policies and procedures can be easily understood and followed. Specific Intel product safety courses include:

**Product Regulations.** The Product Regulations course provides an overview of the laws and regulations that impact Intel Systems products, explaining individual geographical regions' active laws and regulations concerning computer products. It also covers the process by which regulations are developed and revised in each region and the method by which regulations are enforced. The Product Regulations course is intended for personnel on new product planning committees, such as marketing personnel and engineers.

**Product Safety Design.** The Product Safety Design course provides design engineers with an in-depth knowledge of the latest product safety regulations affecting computer products. It is based on Intel's own design checklist, which contains a complete, up-to-date summary of worldwide product safety requirements.

**Product Liability.** This course, based on Intel's Product Liability Audit, is designed to provide employees with an understanding and awareness of product liability issues. The course covers the philosophy behind Intel's commitment to society to build products that are safe and in compliance with applicable regulations, and illustrates this philosophy with real-life product liability cases. The course describes specific methods of reducing risk. It is targeted at a variety of individuals, including those from distributors, factories, small start-up operations, field sales and service and design activities.

**Product Safety Auditors.** The Product Safety Auditors course is provided for individuals in manufacturing, purchasing, component and assembly evaluation, supplier quality assurance and receiving inspection and others who need to be aware of the process of insuring that released products remain safe. Students learn the various certification marks, UL/CSA/TUV inspection practices, documentation, and organization. They also are taught the method for reporting hazards.

## CONCLUSION

Intel takes seriously its responsibility to society to build products that are safe and in compliance with applicable regulations. As a result, our product safety program sets rigorous guidelines from the earliest phases of new product development and extends to well after a product is retired from Intel's active line. Intel employees are trained extensively in product safety issues, since the ultimate responsibility for safe products lies with the individuals involved.







## CHAPTER 5 FIELD ACTIVITIES

### OVERVIEW

The most significant measure of Intel's success in designing, producing and delivering high quality products is the opinion of our customers. To continuously measure our performance from the customers' perspective we have established Customer Quality Engineering (CQE) in Europe, Japan and the United States.

This chapter highlights the quality activities associated with Intel's commitment to support an ongoing partnership with customers. These activities include the regular surveying of customer quality requirements, auditing the quality of delivered products, providing focus for product corrective actions, and providing customer training in reliability methodologies and electrostatic discharge protection.

### CUSTOMER QUALITY ENGINEERING

Customer Quality Engineering is an integral element of Intel's quality system and customer support activities. We focus on understanding customers' quality requirements and expectations; disseminating such information to appropriate organizations; providing a focal point for customer quality programs and issues; recommending quality and reliability goals based on customer expectations; defining and driving Intel's quality methodologies to achieve the required quality goals; and providing direct customer consulting and training in the areas of component electrostatic discharge (ESD) protection, mean time between failure (MTBF) prediction and quality cost factors useful in product make-versus-buy decisions.

### CUSTOMER SUPPORT CENTERS

Customer Support Centers are specially staffed technical groups located in Japan, England and the United States. The Customer Quality Engineers at these sites provide local single-point interfaces between Intel and its customers in that part of the world. These centers resolve quality issues requiring technical expertise and also provide local quality training and liaison for our customers. Corporate Quality and Reliability groups are kept informed of customer issues and provide technical and administrative support as necessary. Local quality managers are in place to provide a high level of direct customer support.

### INDICATOR REPORTS

We use several sources of information to compile monthly CQE reports:

**Customer service installations.** Each time an Intel Systems product is installed we collect quality data. This information is stored in a database maintained by our ASD Worldwide Support service organization headquartered in Phoenix. When we locate defects in delivered products, we correct the deficiency on the spot. Installation data is ultimately passed back to the ap-

propriate Intel site to correct the problem at its source.

**CQE telephone audits.** We monitor and capture field failures to assess the long-term reliability of our products under actual usage conditions. In this way we quickly identify non-predicted failure modes for rapid corrective action.

Each month, CQEs make phone calls to customers to obtain their assessment of Intel product quality. This close customer relationship allows us to determine the delivered acceptance rate for our products. Adverse trends thus become visible and we can then implement corrective action.

Our partnership with customers also enables us to obtain the data necessary to calculate field demonstrated MTBFs for our products. These calculations have a high degree of statistical confidence. We highly value such data; it enables us to ensure that future designs meet the field expectations built up over many years.

Each month, we enter the data from installations, field engineering reports and customer telephone audits into our field quality database, along with comments regarding any problems. This database is then used to prepare our indicator reports.

Indicator reports are prepared for each product line (boards, systems and software) and are presented monthly to the general managers of individual business units. Figure 5-1 shows an example of the graphical quality trend indicator for the MULTIBUS® I business unit products.

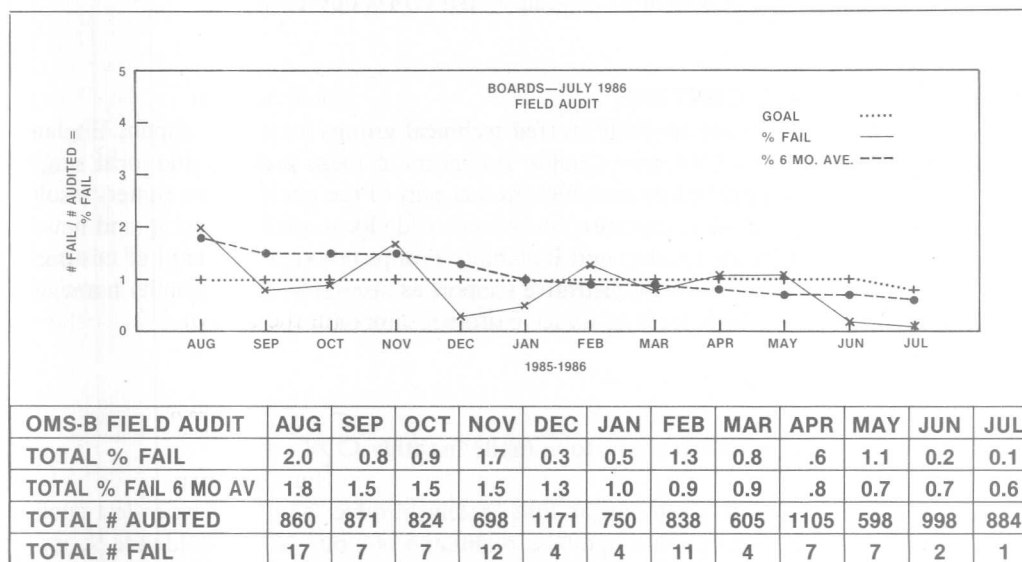


Figure 5-1. Indicator Report for MULTIBUS® I Business Unit Products

The data is summarized in both tabular and graphical formats. It is plotted over a six-month rolling average along with the actual monthly data. The current quality goal for that product line is established by the business unit manager, manufacturing and quality assurance.

The monthly indicator report also includes monthly quality audit data on specific products, categorized by production site. At the beginning of each month, CQE presents the previous month's indicator report to each business unit staff for their education and focus on corrective action. Copies are also sent to related departments, such as engineering, marketing, production management and manufacturing site quality assurance, for their ongoing analysis and understanding.

### **WAREHOUSE AUDITS**

As an additional check on outgoing product quality, Intel performs regular warehouse audits on inventoried products. These audits are intended to check our manufacturing process and provide a general indication of what we expect to see in field audits. Warehouse audits are performed by the quality assurance departments on a monthly basis, covering both the workmanship and functional aspects of the product and the warehouse ESD handling, labeling and storage procedures.

First, a random sample of warehoused products is selected. Each product in the sample is given a visual quality examination, which includes inspection of not only the hardware but packaging materials, carton markings, documentation, etc. We match these findings against the control document that defines what should be present, checking that all appropriate inspection stamps are present. The results of the visual inspection are recorded and any defects noted.

Then, functional tests are performed in accordance with the audit operating instructions set forth by our evaluation engineers (see Chapter 2, Reliability). These instructions are derived from the MTBF verification tests run before releasing a design to production. The functional test is run for several hours to determine that the product functions properly and to ascertain that there are no infant mortality problems. Here again, results are recorded and defects noted.

Also, any workmanship or functional defect found during warehouse audits are traced back to the point of origin and the cause of the defect eliminated. This trace may result in a process change (in the case of workmanship) or an engineering change (in the case of design-related problems). See Figure 5-2.

Finally, the processes of the warehouse administration and product handling are audited. Quality auditors verify the presence of specified ESD protective equipment, proper labeling and storage of products, and the effectiveness of product rotation (First-in, first-out).



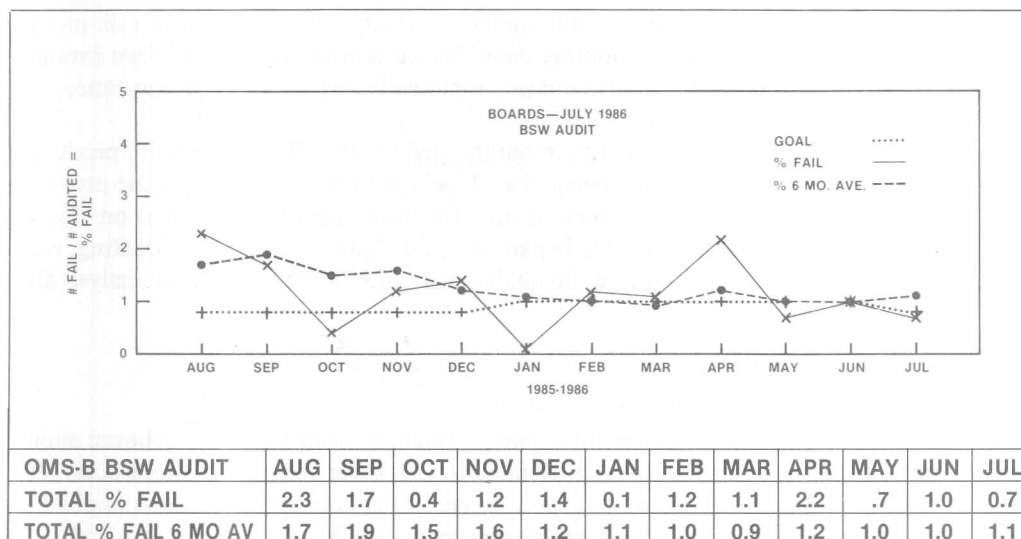


Figure 5-2. Warehouse Audit Report on MULTIBUS® I Product Line

## APPLICATIONS SUPPORT

In some cases, we find that product “defects” are really the consequence of new customer applications, the test results of which were not correlated to our pre-release testing. CQE engineers work closely with customers to identify and resolve application-related issues. CQE will coordinate the problem-solving process that includes using the diagnostic equipment available at our worldwide repair centers or bringing products back to the Systems Group Technical Marketing or Sustaining Engineering groups for detailed Intel engineering support.

## FIELD QUALITY IMPROVEMENT TEAMS

CQE also oversees an activity called the Field Quality Improvement Team (FQIT), responsible for making sure problems discovered in the field are resolved in a timely and satisfactory manner.

Site FQIT teams are chaired by the site quality assurance managers with members from manufacturing, engineering, test engineering and other appropriate departments. The role of the site FQITs is to review corrective action progress, assign priorities and resolve issues.

The corporate FQIT is chaired by the manager of the Systems Group CQEs, with members from all production site quality assurance engineering and business unit engineering departments. This team meets bi-weekly (via teleconference) to oversee the activities of the site FQIT teams, set priorities, and share problems and solutions.

**FIELD RELATIONS**

CQE engineers visit many customers every year, usually accompanied by the account's Field Sales Engineer. We visit accounts to review our quality performance, to resolve outstanding issues and to plan ongoing improvement programs. These visits keep us in close touch with our customers and allows us to continually improve quality through open communications.

**CONCLUSION**

To be our customers' supplier of choice, Intel must provide the very highest quality products. Ongoing customer feedback is the best way to gauge our success in this area. We value customer feedback and seek it at every opportunity to ensure our long-term relationships.

Customer Quality Engineers serve as Intel's "antennae" for measuring our quality performance with customers and reporting the results directly to management. Customer Quality Engineers also serve as ombudsmen for Intel customers, fielding any and all quality issues and tracking down resolutions.

Through our Customer Quality Engineers, our worldwide Customer Support Centers and our commitment to providing quality training, the field activities of Intel are designed to be a working partnership created to make our company and yours more profitable on a long-term basis.







## CHAPTER 6 SUPPORT

Intel maintains a Total Quality Assurance program to ensure its products and services continuously meet the customer's requirements. Every employee at Intel is committed to doing a quality job, therefore, many supporting quality activities are performed by company functions other than the direct quality department.

This section highlights the quality programs of several supporting groups. These groups are responsible for the areas of component qualification, peripherals and power supply qualification, engineering and manufacturing documentation, customer service and training, and compliance with customer contracts.

### **CORPORATE COMPONENTS ENGINEERING**

Corporate Components Engineering (CCE) assures that all commercial components used in Intel Systems Products are properly selected, analyzed, specified, and documented with respect to technology, reliability, safety, and fitness for use. CCE evaluates all new components before they're integrated into product design and serves as a technical resource for component application assistance.

Corporate Components Engineering is comprised of electronic and mechanical engineers who specialize in component evaluation and specification. A CCE representative is included on all product development teams to provide application assistance and qualification support, resolve component technology requirements with suppliers, and support manufacturing with component failure analysis.

### **Commercial Part Drawing**

Corporate Component Engineering's activities begin with an engineering request for approval of a commercial part. CCE first determines the commercial suppliers for the part, then obtains samples and subjects them to extensive qualification testing. After successful testing, the part is approved for design and manufacturing. CCE issues a Commercial Part Drawing (CPD) that specifies all component requirements, including safety or regulatory compliance, dimensions, mechanical and electrical characteristics, functionality, operating environment and quality assurance requirements.

### **Part Substitutions**

CCE also maintains control over commercial part substitutions that occur as a result of supplier shortages. Only upgrading of parts is allowed; i.e., to better packaging (ceramic vs. plastic), better reliability (MIL-spec vs. commercial) or better tolerance (tighter vs. looser). CCE currently allows substitutions only in the following commodities: burned-in commercial logic devices, capacitors (fixed), resistors (fixed), Intel components, and acceptable military counterparts.

### Common Design Parts Catalog

All commercial parts judged to be either acceptable or recommended for use in Intel products are listed in a CEE common design parts catalog. This catalog contains only parts that have an Intel Systems Commercial Part Drawing (CPD) available in the document control centers and have completed evaluation and qualification.

### Qualification

Corporate Components Engineering provides both electrical and mechanical device evaluation and qualification testing, assuring that commercial parts used in Intel systems products meet specification at both the component and systems level. Wherever applicable, CCE bases its testing on military specifications (such as MIL 883) and commercial standards (such as those from the American National Standards Institute, Underwriters Laboratories and the Canadian Standards Association). A typical qualification test plan for IC packages is shown in Table 6-1.



Table 6-1. Component Qualification Test Plans

COMPONENT QUALIFICATION PLANS							
IC PACKAGES							
109922, REV. 8							
5.3 TABLE . Qualification Test Matrix:							
.1 GROUP I - VENDOR DATA							
Title	Test Method <sup>1</sup>	Stress	Package <sup>2</sup>	SS/AL/ALS <sup>3</sup>	Read Out	Accept/Reject	End Point
Dimensions	Note 4		H, NH	50/1/3	1	0/1	Visual, CPO Tolerance
Marking Permanency	2015C	Chemical	H, NH	50/1/3	1	0/1	Visual
Lead Integrity <sup>5</sup>	200482	Fatigue	H, NH	30/1/3	1	0/1	
Solderability	2003	100°C	H, NH	80/1/3	1 hr. of aging	0/1	Visual, 90% Lead Coverage
Wire Bond Integrity	20110	Bond Pull	H, NH	200/1/3 Wires	To destruction	1/2	>2g AL Wires >3g AU Wires
Die Adhesion	2019	Die Shear	H, NH	50/1/3	To destruction	0/1	>2.5K PSI
Mechanical Series	20028 2007A 2001	Shock Vibration Centrifuge <sup>6</sup>	H	50/1/3	Y1-Orientation	1/2	Electrical, Visual, Die Adhesion
Salt Spray	1009A	35°C	H, NH	50/1/3	24 hrs.	1/2	Visual
.2 Group II - Vendor And/Or Intel Data							
Title	Test Method <sup>1</sup>	Stress	Package <sup>2</sup>	SS/AL/ALS <sup>3</sup>	Read Out	Accept/Reject	End Point
Humidity	Alternate	85°C/85%RH, Pin Bias	NH	100/1/3	1000 hrs	<0.8%/1 Khr at 85/86	Electrical, Visual
Saturated Steam		121°C/100% RH/2 ATM No Bias	NH	50/1/3	96 hrs	≤2% at 121°C/ 100% RH/ 2 ATM	Electrical, Visual
Temperature Cycle	1010C	-65°C to + 150°C	H, NH	50/1/3	1000 cycles	<3% at 1000 cycles Cumulative	Electrical, Visual
Thermal Shock	1011C	-65°C to + 150°C	H, NH	50/1/3	200 cycles	<2% at 200 Cycles Cumulative	Hermetic, Bonds

## NOTES:

1. All test methods are as specified in MIL-STD-883, unless otherwise specified.
2. Package types: H = Hermetic; NH = Non-hermetic.
3. SS/AL/ALS = Sample Size per Assembly Lot per Assembly Lots.
4. Dimensions are to be verified per the component Commercial Part Drawing (CPD).
5. This test does not apply to PLCC package technology.
6. This test parameter is a function of die size/package size.

AML Status: The package qualification shall be a concurrent activity with the die qualification of a device. The device is required to pass both a package and die qualification before a status of "C" or "A" can be assigned. Failure to pass the package qualification shall result in a "D" (Disapproved Status).

Die Revisions: Die revisions are subject to re-qualification. If the changes do not effect final die passivation or otherwise effect package quality or reliability, the package re-qualification is waived.

### Laboratory Facilities

CCE uses both Intel component failure analysis laboratories and commercial test houses to perform qualification testing. Vendor-supplied test or reliability data may also be accepted, with CCE's approval.

Intel laboratories contain the full range of equipment required to test semiconductor devices for functionality, packaging and die-level defects, including parametric testers, probes, package hermeticity testers and scanning electron microscopes. They also allow a broad range of electrical and mechanical tests through tensile testers, environmental shock/vibration/humidity/temperature cycle testers, electrostatic discharge (ESD) testers and general-purpose microscopes. See Figures 6-1 to 6-6.



Figure 6-1. VLSI 60-Pin Component Tester

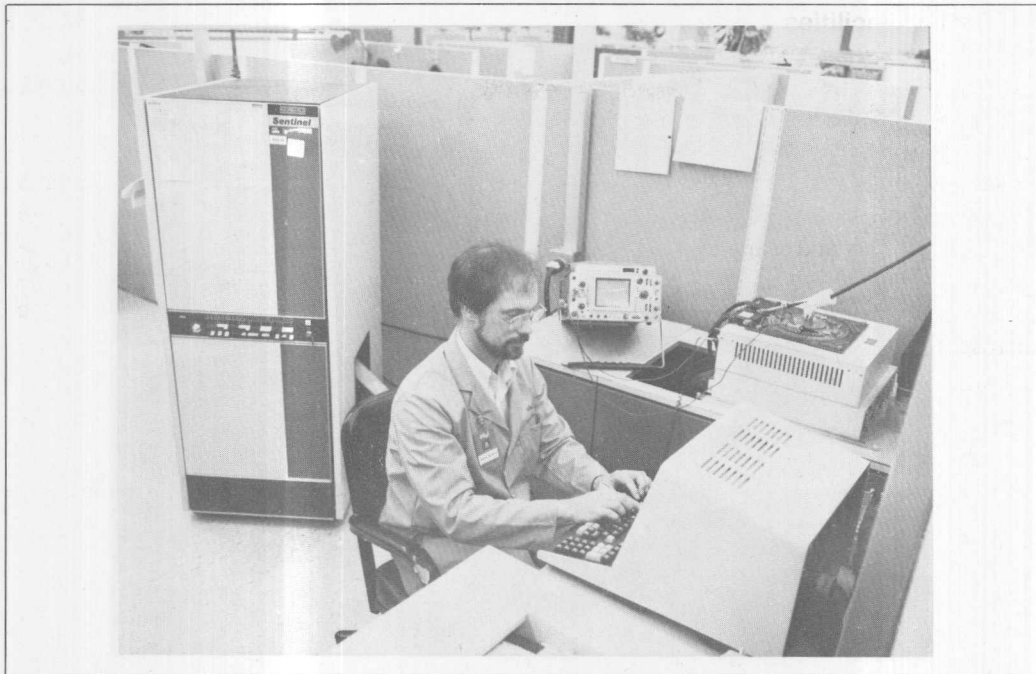


Figure 6-2. Automated Digital Logic Tester

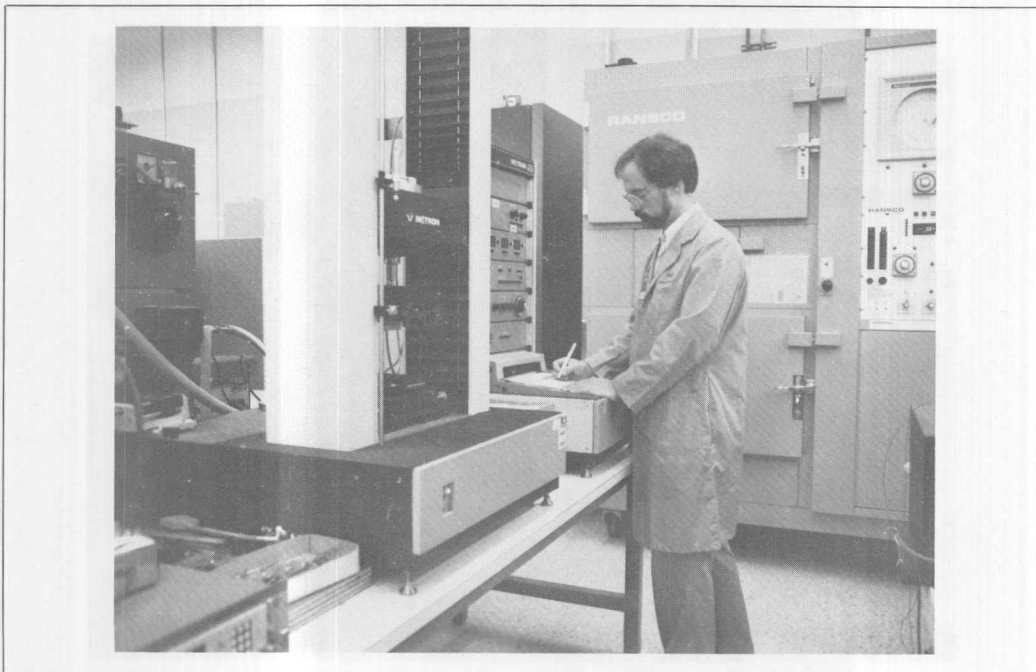


Figure 6-3. Programmable Force-Displacement Connect Tester



Figure 6-4. ASIC 256-Pin Tester



Figure 6-5. GPIB Automated Oscillator and Passive Test Lab

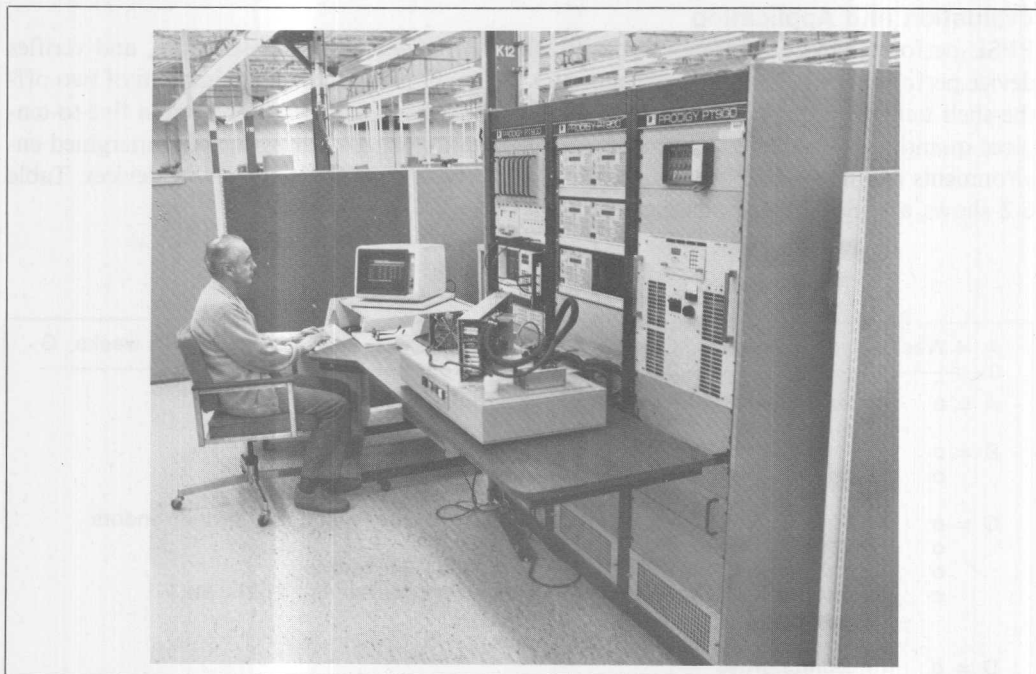


Figure 6-6. ATE Power Supply Dynamic Test Lab

## PERIPHERALS AND POWER SUPPLY ENGINEERING

The Peripherals and Power Supply Engineering (PPSE) group selects and qualifies mass storage peripheral devices and power supplies used in Intel systems products. PPSE engineers are experts in the selection, qualification, application engineering, and supplier relationships in these commodities.

PPSE engineering activities include an ongoing focus on establishing and supporting controller interface standards, such as ST 506/412 and ESDI (Winchester disk); SA 450/460/475 (flexible disk); Q1C-02 (1/4 inch streaming tape); ANSI X3T9/1226 (standard interface), and Serial OEM Interface (SOEMI). PPSE is represented on the ANSI subcommittees for ANSI Intelligent Peripheral Interface IPI X3T9.3 and ANSI Small Computer Systems Interface SCSI X3T9.2.

### Device Qualification

PPSE tests devices in a custom environmental chamber to characterize their operational performance. The results of these tests statistically demonstrate the device's adherence to the supplier's specifications. If the device fails to meet or marginally meets specification, PPSE negotiates with the supplier to change the device design or manufacturing process to meet specification.

### Evaluation and Application

PPSE performs device reliability demonstration testing, develops test software, and verifies device performance in intended application(s). Evaluations begin with a minimum of two off-the-shelf units from potential suppliers. Successful products are then reordered in five-to-ten-piece quantities for more comprehensive qualification testing. Testing includes margined environments and mean time between failure (MTBF) validation for high-volume devices. Table 6-2 shows a typical device qualification time line.

**Table 6-2. Typical Device Qualification Time Line**

A	4 Weeks	B	2 Weeks	C	4 Weeks	D	1 week	E	4 Weeks	F	n weeks	G
0	-----	0	-----	0	-----	0	-----	0	-----	0	-----	
A =	o	Order Preliminary Evaluation Units from Candidate Vendors										
B =	o	2 Preliminary units arrive										
	o	Begin Preliminary Evaluation										
C =	o	Preliminary Evaluation Complete; select 1-2 most promising device vendors										
	o	Order 5/10 Engineering Analysis Units										
	o	Begin Preliminary SGPO System Integration Evaluation										
	o	Initiate vendor review (history, survey if appropriate, financials, etc.) if necessary										
D =	o	5/10 Units arrive										
	o	Preliminary Source/IQC tests released										
	o	SGPO Preliminary System Integration Evaluation completed										
	o	Nominal Environment Baseline Device Test completed										
E =	o	Begin 4 week Engineering Analysis and Margined Environment testing										
	o	Vendor review data collected										
F =	o	Testing completed										
	o	Vendor review data analyzed and results available										
	o	Source/go/no-go decision for AML entry and initiation of system integration										
	o	IQC tests/procedures released										
G =	o	Accumulate MTBF data										

★ 15 Week Qualification Cycle (for "Good" Devices)

★ Duration of Qualification Cycle Extends if problems requiring vendor correction encountered

★ "High" Volume Devices (>2500/YR) Require MTBF Validation (60% CL) prior to AML entry or initiation of system integration.



## Reliability Testing

PPSE writes an overall reliability test plan for each device family. During the reliability test, the devices are exercised comprehensively and monitored to verify functionality and error rates for specified MTBF validation. Table 6-3 shows the scope of a typical Winchester drive reliability test plan.

Table 6-3. Peripheral Reliability Test Plan for Winchester Disk Drive

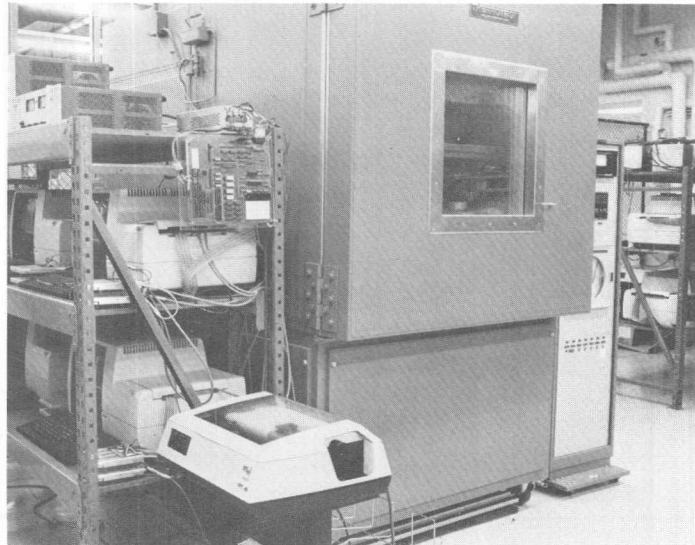
TABLE OF CONTENTS
SCOPE
TEST PURPOSE
Reliability Tests
Disk Error
Environmental Test
Functional Spec. Compliance Test
Auxilliary Tests
Vibration Test
Drop Test
Storage Test
Electrostatic Discharge Test
Acoustical Noise Test
RELATED DOCUMENTS
GENERAL RELIABILITY TEST SEQUENCE
Shakedown Test
Formatting Drives
Handling Defective Tracks
MTBF Testing
Description of Tests Performed
Weekly Duty Cycle
EQUIPMENT / MATERIALS
Major Items
Consumables
FAILURE DEFINITION
Catastrophic
Inconvenience
External
Indeterminate
Additional Media Defects
Failure Weighting System
TEST REPORTS
Test Log
Test Station Log
Failure Report
Final Report
Test Progress Report
GENERAL TEST SCHEDULES
Total Test Length / Time



The peripheral's reliability test utilizes Intel products such as the Series III/IV Development Systems, iSBC®-214 and 215D Peripheral Controllers, and iSBC®-544 Intelligent Communications Controllers in a highly automated test system environment. (See Figures 6-7 and 6-8.) The typical test station setup is depicted in Figure 6-9.



**Figure 6-7. Intel Series IV Lab Control System**



**Figure 6-8. Peripherals Environmental Test Lab**

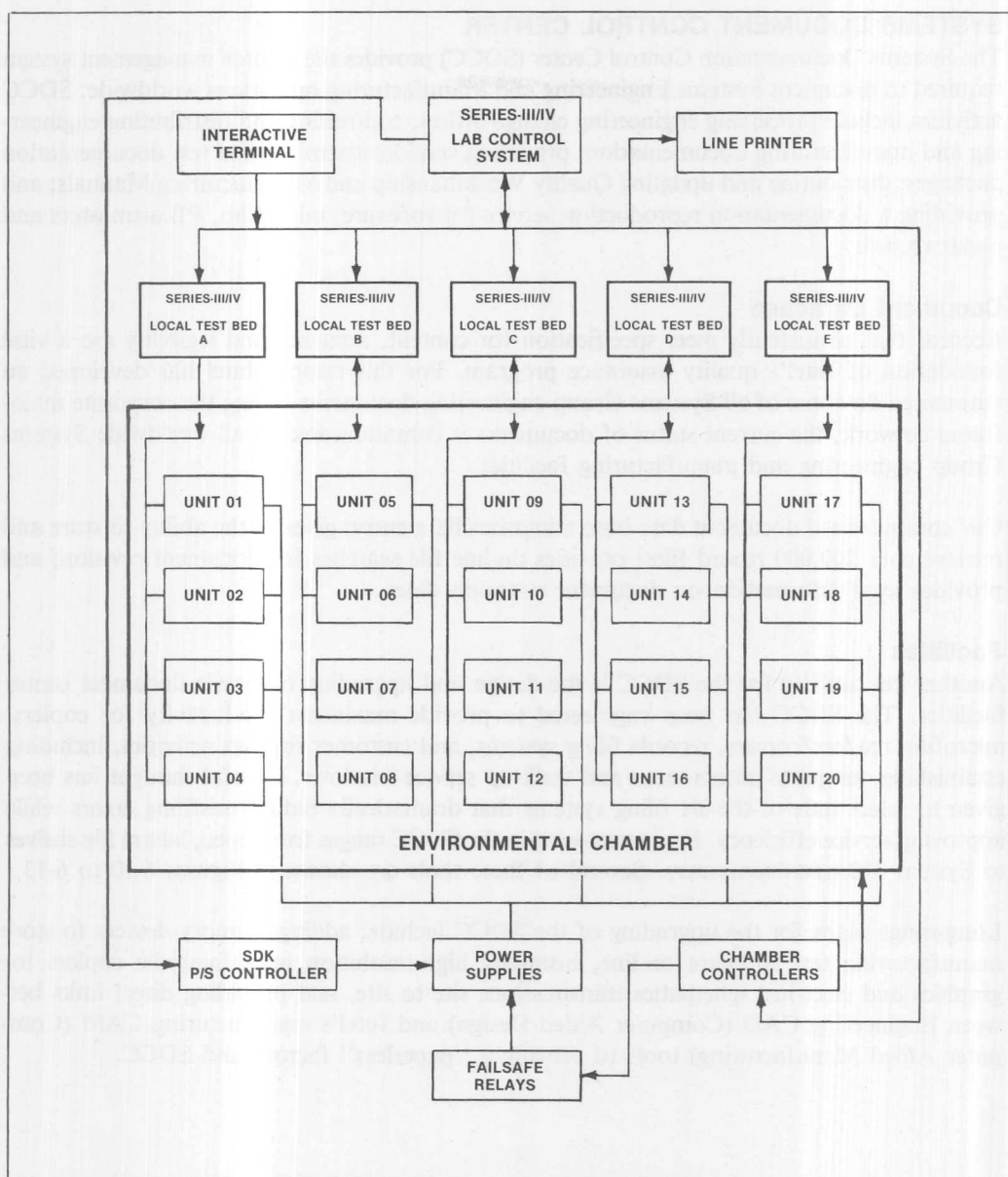


Figure 6-9. Test Station Set-Up Block Diagram

Power supply characterization is done using the 3H PT900 ATE test equipment for both linear and switcher devices. The lab is also equipped with a 100-point data-logger, environmental ovens, numerous solid-state loads and an IEEE 587 power line surge tester.

## **SYSTEMS DOCUMENT CONTROL CENTER**

The Systems Documentation Control Center (SDCC) provides the records management system required to document Systems Engineering and Manufacturing operations worldwide. SDCC activities include processing engineering change orders; controlling and distributing engineering and manufacturing documentation; providing vendor, assembly, and test documentation packages; distributing and updating Quality Workmanship and Manufacturing Manuals; and providing a documentation reproduction service for software, microfilm, PB artmasters and paper records.

### **Document Database**

Records that consistently meet specification for content, accuracy and legibility are a vital foundation of Intel's quality assurance program. For this reason, Intel has developed an automated database of all Systems Group engineering documents. Using the corporate main-frame network, the current status of documents is communicated to all worldwide Systems Group engineering and manufacturing facilities.

Our computerized document data base minimizes data entry; gives us the ability to store and retrieve over 200,000 record files; provides on-line file searches for document revision; and provides legal information on document retention dates.

### **Facilities**

Another key activity for the SDCC is the design and upgrading of Intel's document center facilities. The SDCC has been engineered to provide maximum productivity for copiers, microfilm readers/copiers, records filing systems, and customer support activities, including establishing computer access areas and walk-up service windows. Careful thought has been given to select state-of-the-art filing systems that dramatically reduce misfiling errors while improving service efficiency. Equipment used in the SDCC ranges from open, lateral file shelves to System 310 microcomputers. Several of these tools are shown in Figures 6-10 to 6-13.

Long-range plans for the upgrading of the SDCC include: adding memory devices to store manufacturing test software on-line, installing high-resolution microfacsimile copiers for graphics and electrical schematics transmissions site to site, and providing direct links between Engineering CAD (Computer Aided Design) and Intel's manufacturing CAM (Computer Aided Manufacturing) tools to provide a "paperless" factory and SDCC.



Figure 6-10. State-of-the-Art Terminal Digit Files

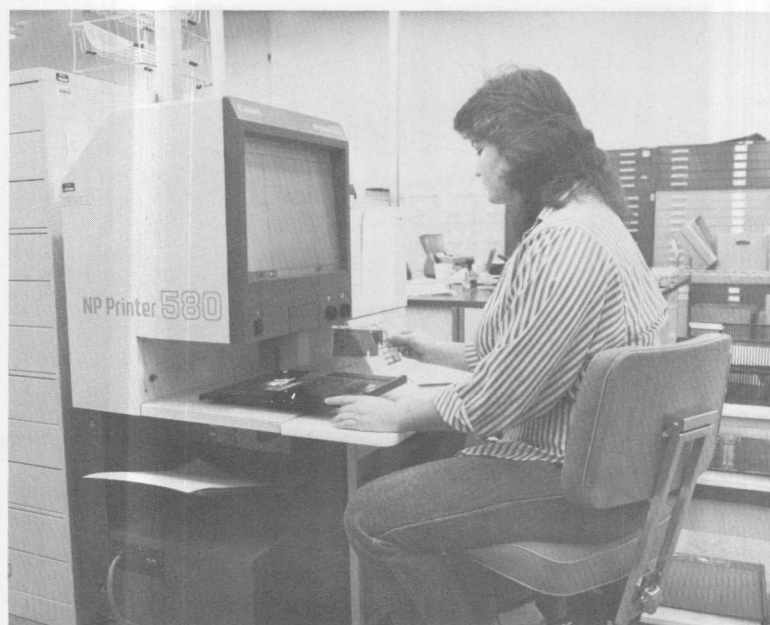


Figure 6-11. Automated Microfiche Reader/Printer



**Figure 6-12. Manufacturing Assembly Instructions Being Color-Copied**



**Figure 6-13. Customized Storage of Product Test Software**

### ASD:WORLDWIDE SUPPORT

Intel's ASD:Worldwide Support assures that customers are offered a wide range of pre- and post-sales services, including product application and installation training; product installation and field maintenance services; product warranty and repair support; system integration support agreements for OEMs and volume end users; software subscriptions and update packages; and a library of customer-submitted software programs.

The ASD:Worldwide Support organization is comprised of hardware and software engineers, product training specialists and administrative staff specializing in support services. These engineers are technical experts on Intel products and also provide support for other companies' computers and peripherals integrated into Intel products.

ASD:Worldwide Support has technical centers in Arizona, California, England, Japan and Hong Kong. Figure 6-14 shows Intel's full range of customer support services.

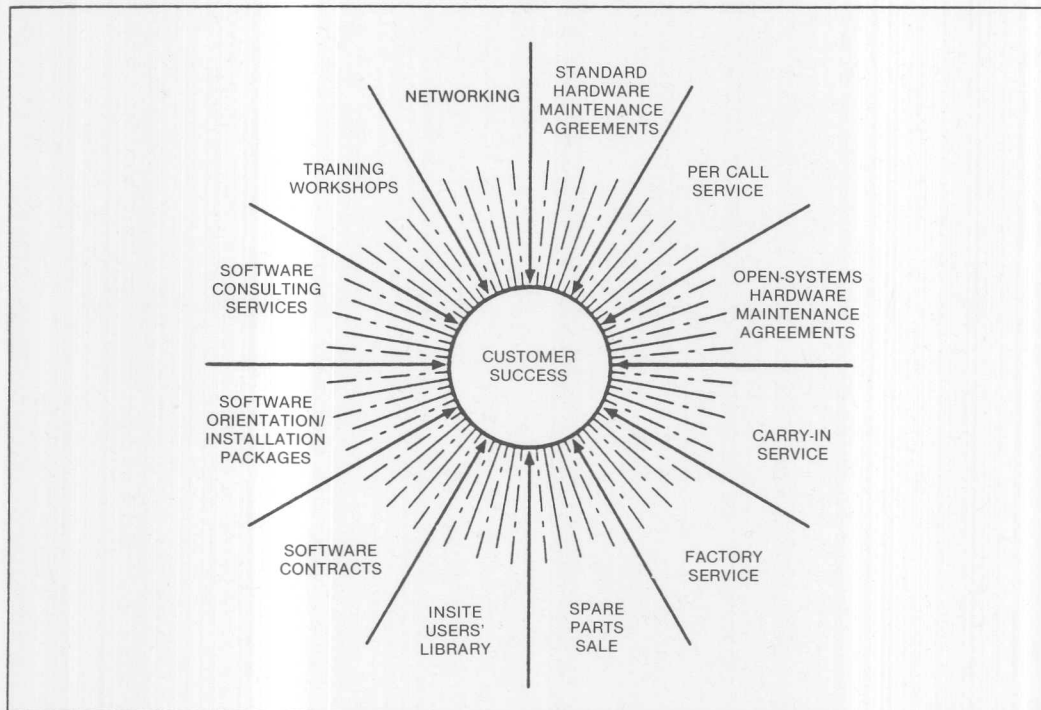


Figure 6-14. Full Range of Support Services

Matching Intel's service to its technology requires the major activities of hardware support, software support, customer training and several field quality programs.

**Hardware Support Services**

Hardware support services include initial product installation and warranty, long-term maintenance agreements, and selected support for non-Intel products. ASD:Worldwide Support engineers maintain and repair products either at Intel repair centers or on-site at the customer's facility. Quality assurance activities include the use of calibrated test equipment, the installation of authorized factory spare parts, providing hardware diagnostics and tests to assure the repaired product meets specifications, and maintaining a comprehensive computerized database containing product component failure information. Table 6-4 highlights Intel's various service agreements.

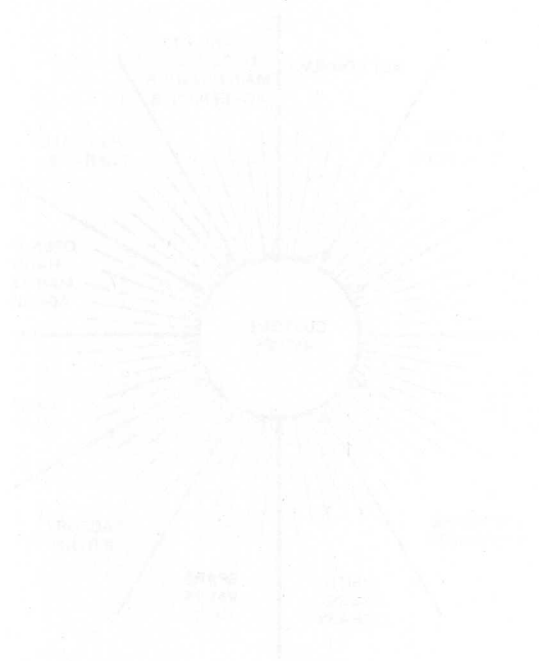




Table 6-4. Hardware Support Offerings

Service	Highlights
Standard Hardware Maintenance Agreement	<ul style="list-style-type: none"> <li>• Full level service covering parts, labor, preventative maintenance and engineering change installations at the customer site.</li> <li>• Customer selects hours of coverage.</li> <li>• Applies to standard Intel products.</li> </ul>
Carry-in Maintenance Agreement	<ul style="list-style-type: none"> <li>• Economical</li> <li>• Same service as standard contract, but the customer delivers the equipment to an Intel facility.</li> </ul>
Per Call Services	<ul style="list-style-type: none"> <li>• Purchase labor and materials on an as-needed basis for installations, repairs, preventative maintenance, and other services.</li> </ul>
Factory Services Factory Direct Return Authorization Service (DRA)  Factory Return Replacement Authorization Service (RRA)	<ul style="list-style-type: none"> <li>• Economical 30-day turnaround</li> <li>• Applies to board level products in all areas and system customers in non-serviceable areas.</li> <li>• Expedited service 48-hour turnaround</li> <li>• Applied to currently manufactured board level products in minimal quantities.</li> </ul>
Installation and Warranty	<ul style="list-style-type: none"> <li>• Installation is included on many Intel system products. Hardware support initials, services and verifies correct operation before turning the system over to the customer.</li> <li>• Warranty service is provided either via factory returns or at the customer site, depending on the warranty associated with that particular product.</li> </ul>
Open Systems Support	<ul style="list-style-type: none"> <li>• Individually tailored contracts to meet unique equipment configurations and customer support needs.</li> <li>• Can include support for non-Intel products as part of the total support agreement.</li> <li>• Provides the international service capabilities on Intel's Hardware support organization to the end-user customer of System Integrators and OEMs.</li> </ul>

Not all services provided for all product lines. Contact your local Intel service office for more specific information on the right service to meet your needs.

### Software Support Services

Software Support provides a comprehensive range of post-sales support programs for both Intel software and third-party software marketed by Intel. Services include establishing soft-

ware support contracts, updating software revisions, providing technical applications engineering, and maintaining a customer-developed software library program.

Quality assurance activities include updating diskettes, tapes, manuals and documentation; documenting product problems and solutions; providing technical assistance to Intel's software engineering staff; and providing on-site customer assistance. Figures 6-15, 6-16 and 6-17 are flow charts for major quality assurance activities: updates, software problem reporting (SPR) and our technical information phone service (TIPS).

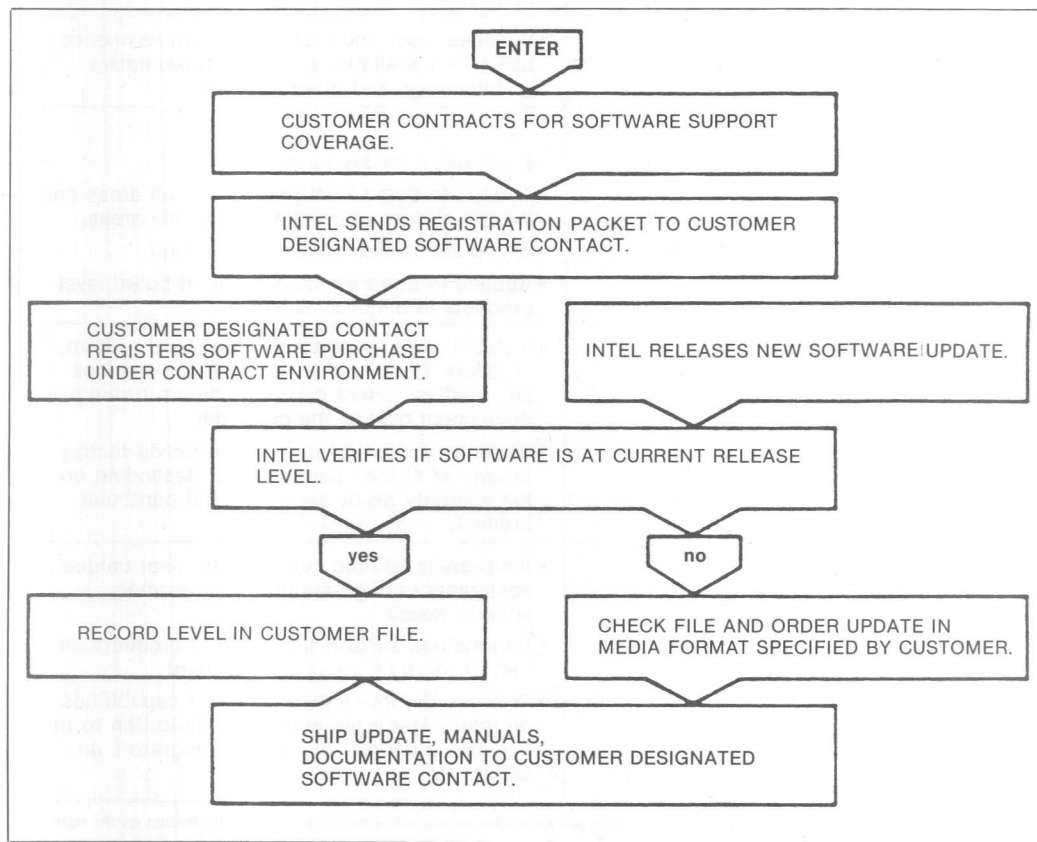


Figure 6-15. Software Update Flow Chart

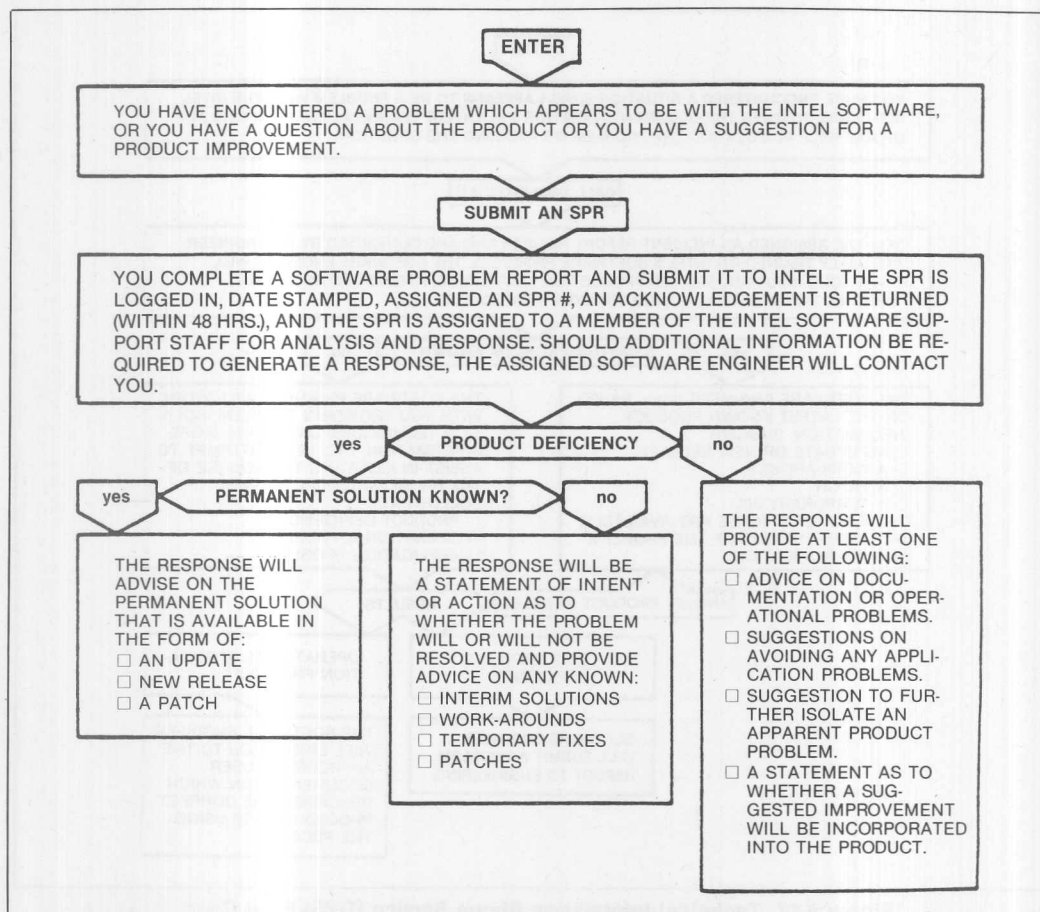


Figure 6-16. Software Problem Report (SPR) Flow Chart

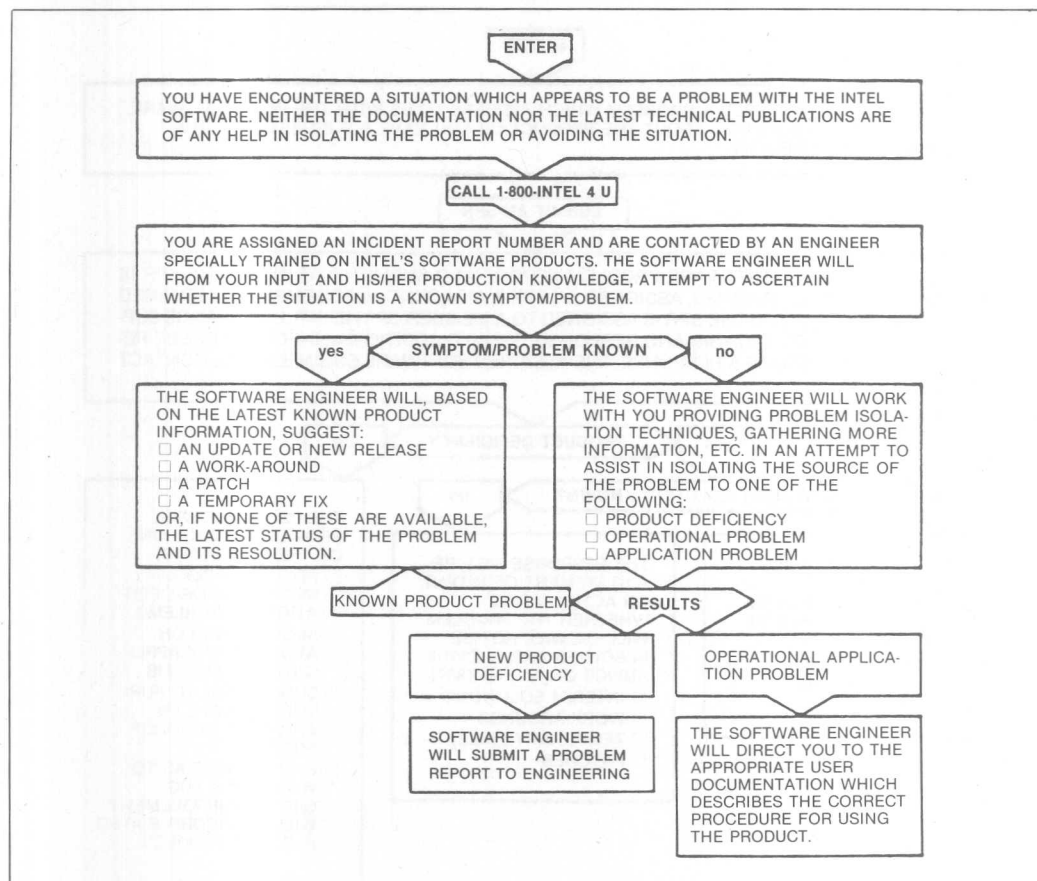


Figure 6-17. Technical Information Phone Service (TIPS) Flow Chart

When you call TIP Service, the receptionist initiates a numbered incident report and provides you with this assigned number for future reference. At this point you will be able to speak with a member of Intel's Software Engineering staff. If a representative is not immediately available, the call will be returned within two hours to assure prompt resolution of your concern.

### Customer Training

Intel conducts training workshops on a wide range of microcomputer and data base management products. The workshops are held regularly at Intel training centers across the United States, Europe and Japan. They may also be held at customer sites, on request. Training is an integral aspect of Intel's total quality assurance program to ensure Intel remains the customer's preferred supplier.

Training workshops give customers hands-on experience in a structured laboratory environment taught with slide/video presentations and student reference manuals. Workshops are targeted at design engineers, but they've also been very useful to evaluation engineers, technical writers and engineering management.

Workshops typically span three to nine days. A sample course outline (shown in Figure 6-18) demonstrates the scope of instruction as well as the frequency of lab sessions. A sample of customer training courses (Table 6-5) shows the broad support offered to customers, including basics of microprocessor data communications, software techniques, and tools for hardware and software emulation to debug new designs.

<b>Module Name:</b>	80186 Peripherals
<b>Description:</b>	This module will demonstrate how to program the 80186 and 80C186 internal peripherals.
<b>Class Size:</b>	16 Students
<b>Duration:</b>	11 Hours
<b>Attendee Profile:</b>	This class is for design engineers and programmers who will be writing programs using the 80186 or 80188.
<b>Prerequisites:</b>	Prior experience in assembly language for the Intel 16-bit microprocessor family along with the enhanced instructions of the 80186 are required. The 8086 and 80286 Real Mode Programming workshop and 80186 Overview satisfy these requirements.
<b>Objectives:</b>	<p>The student will program the 80186 internal peripherals. To accomplish this, the student will:</p> <ol style="list-style-type: none"><li>1. Program the relocation registers, chip selects and wait states.</li><li>2. Set up the timers to provide a specified count.</li><li>3. Initialize the Internal Interrupt controller.</li><li>4. Generate DMA transfers from memory to I/O.</li><li>5. Use the 80C186's and 80C188's new features.</li></ol>
<b>Module Outline:</b>	<ul style="list-style-type: none"><li>• 80186 Control Block, Chip Select Unit and Wait State Generator<ul style="list-style-type: none"><li>— Peripheral Control Block</li><li>— Relocation Register</li><li>— Relocation Register Exercise</li><li>— Memory Chip Select Registers</li><li>— Peripheral Chip Select</li><li>— Setting up Chip Select Logic Exercise</li></ul></li><li>• The 80186 Timers<ul style="list-style-type: none"><li>— Timer Features</li><li>— Timer 0 and Timer 1</li><li>— Timer 2</li><li>— Setting up the Timers Exercise</li></ul></li><li>• The DMA Controller<ul style="list-style-type: none"><li>— 80186 DMA Controller Features</li><li>— DMA Motivation</li><li>— DMA Controller Registers</li><li>— Exercise</li><li>— DMA Controller Exercise</li></ul></li><li>• The Interrupt Controller<ul style="list-style-type: none"><li>— The Interrupt Control Unit</li><li>— Programming the Interrupt Unit</li><li>— Interrupt Control Block Exercise</li></ul></li><li>• The 80C186 and 80C188<ul style="list-style-type: none"><li>— Features of the 80C86 and 80C188</li><li>— 80C186 and 80C188 New Features</li><li>— Exercise</li><li>— 80C186 and 80C188 Tools</li></ul></li><li>• Lab Exercises<ul style="list-style-type: none"><li>— Using the DMA Controller</li><li>— The Interrupt Controller</li></ul></li></ul>

Figure 6-18. Sample Course Outline

Table 6-5. Customer Training Courses

COURSE TITLE	DESCRIPTION
Introductory: Self Study Introduction Microprocessors	Contains an 8085-based kit, audio cassettes, workbook, and manuals.
Introduction to Micro- processors Using the 8086	Covers fundamental computer concepts as they relate to the 8086.
<b>Microprocessors and microcontrollers:</b>	
8086 & 80286 Real Mode Programming	Architecture, assembly language programming for 8086 & 80286, real mode operations of 80286.
80186 Microprocessors	Programming of integrated 80186 peripherals, Instruction set, Intel development tools for DOS-based personal computers.
Intel Numeric Coprocessors	Architecture, programming for 8087 and 80287.
80286 Microprocessors	Architecture, programming for 8087 and 80287.
Operating System Concepts for the 80286	80286 overview and tools, tables and descriptors, Using the operating system writing considerations.
80386 ASM for 8086 Programmers	80386 programming models, instruction sets, addressing modes and data types.
80386 System Software	32-bit operating system environments and implementation on 80386.
80386 System Hardware Design	Designs of 80386 base systems, interfaces to 80387 Design numeric co-processor, 82385 cache controller, 82380 DMA controller, 82786 graphics co-processor and 82586 LAN co-processors.
MOS 8085 Microprocessors	Architecture, assembly language programming: in-circuit emulator useage.
1CE™ User's	Debug hardware by breakpoint capabilities, real-time emulation, analyze and debug software at high level and assembly level languages.
MCS®-51 Microcontrollers	Architecture including I/O, timers/interrupts, Boolean processor and memory types. Assembly language programming.
MCS®-96 16 Bit	Architecture and programming of 8098 family. Functions of I/O, timers, converters and controller applications.
BITBUST™	Distributed Control Modules and support software. Remote control and monitoring.
<b>Operating Systems and Programming Workshops</b>	
PL/M Programming	PL/M programming techniques, concepts of block structure, language syntax and structure.
IRMX® 86 Operating System	Two part workshop on IRMX® 86, Rel. 7, real-time multi-tasking executive principles and implementation. Techniques needed to design and implement software using the PL/M language for the family of microprocessors. Introduction of IRMX® 286 and protection mechanism is discussed.



Table 6-5. Customer Training Courses (Continued)

COURSE TITLE	DESCRIPTION
IRMX® 286 Operating System	Compatibility of IRMX® 86 and IRMX® 286 program development and porting software to IRMX® 286.
XENIX Fundamentals	XENIX Release 3.4 commands, file system visual editor, directories and communication with other users.
XENIX Shell Programming	Write shell programs using variables, keywords, pipelines and debugging aids.
XENIX System Administration	Installation, configuration and administration of XENIX system
Introduction to "C"	Write, debug and execute "C" programs. Utilize "C" data types including structures and pointers.
System Programming in "C"	Utilization of screen processing, program maintenance, process control, pipes, signals, locks, memory allocation and shared data segments.
<b>Local Area Networking Workshops</b>	
Local Area Networks Overview	Computer networks concepts, communication protocols, (ISO-OSI model), media, topologies and access methods. Introduction to MAP.
INA 960	INA 960 in OpenNET™ and ISO-OSI model. Layout, interfaces and design principles of INA 960.
RMXNET	RMXNET in OpenNET™ and ISO-OSI model. Principles of RMXNET administration of networks and configuration and tuning of systems.
XENIX-NET Applications	XENIX-NET features and writing custom applications between XENIX systems and OpenNET LAN.
<b>Office Automation Workshops</b>	
Office Automation Introduction	Introduction to applications such as word processing, spreadsheets, databases and graphics packages.
Office Automation Advanced	In-depth advanced training on office automation packages and creation of databases and spreadsheets.
IDIS System Administration	Utilizing XENIX fundamentals with IDIS Rel. 2.0 Key Operator commands to perform system administration tasks.
XENIX System Administration	Two part workshop utilizing XENIX Rel. 3.4 commands to install, configure and implement a XENIX system. Advance workshop also covers external 310 communications.
IDIST™ Network Administration	IDIS configuration, installation, operation and maintenance of Intel 310 and PC network.
XENIX Network Administration	XENIX configuration, installation, operation and maintenance of Intel 310 and PC network.

\* XENIX is a registered trademark of Digital Equipment Corporation.

**Field Quality Programs**

The Customer Support Operation has several programs aimed at assuring that customers continue to receive high-quality products and services from Intel. The first is a quality monitoring and control program based on installation data. Quality data gathered at the time of installation is kept in a central database and used to establish trends of functional and non-functional (workmanship) product defects.

The second field quality program is a formal quality audit to obtain first-hand field quality data. This audit is supplemented by periodic third-party audits conducted for Intel by professional customer survey companies. Both audits are intended to provide Intel with information leading to improvement in the services of the ASD:Worldwide Support organization.

The third field quality program is the rigorous collection and analysis of product failures. Data from CSO repair centers is collected on part types, manufacturers, application and cause of failure. Failure analysis gives Intel insight into the factory, design or raw material supplier processes that must be improved to progress towards our goal of defect-free products.

**CONTRACT REVIEW**

Customer Quality Engineering has the responsibility of reviewing and approving all customer contracts for quality and reliability requirements and assuring that both Systems corporate-level and manufacturing site-specific programs comply with the contracts.

CQE has a team of managers and engineers who specialize in reviewing contracts to assure reliability, safety and regulatory agency compliance, quality program levels (MIL-Q-9858, ANSI Z 1.15, FAR52.246-2, NASA 5300.4, commercial), and environmental conditions. Table 6-6 contains a partial listing of U.S. and international quality/reliability specifications met by Intel.

Table 6-6. Partial Listing of Contractual Specifications for Quality and Reliability

CUSTOMER	REQUIREMENT	TITLE
Military/ Aerospace	MIL-Q-9858A	Quality Program Requirements
	MIL-STD-105D	Sampling Procedures and Tables for inspection by attributes.
	MIL-STD-414	Sampling Procedures and Tables for inspection by variables.
	MIL-STD-120	Gage inspection.
	MIL-STD-202E	Test methods for electronic and electrical component parts.
	MIL-STD-461B	Electromagnetic emission and susceptibility requirements for the control of electromagnetic interference.
	DOD-STD-1686 & DOD-HDBK-263	Electrostatic discharge control program for protection of electrical and electronic parts, assemblies and equipment (including electrically initiated explosive devices).
	MIL-1-45208A	Inspection system requirements.
	MIL-C-45662	Calibration system requirements.
	MIL-STD-1472B	Human engineering design criteria for military systems, equipment and facilities.
	MIL-STD-1562C	Lists of standard microcircuits.
	MIL-STD-781B	Reliability tests: exponential distribution.
	RADC-AD-821640	RADC reliability notebook.
	MIL-STD-217D	Reliability prediction of electronic equipment.
	MIL-STD-756	Reliability prediction.
	MIL-STD-785	Requirements for reliability program (for systems and equipments).
	MIL-STD-839	Parts with established reliability levels, selection and use of.
	MIL-HDBK-217	Reliability stress and failure rate data for electronic equipment.
	MIL-STD-810D	Environmental test methods and engineering guidelines.
Commercial	H-50	Evaluation of a contractor's quality program.
	H-106	Multi-level continuous sampling procedures and tables for inspection by attributes.
	H-108	Sampling procedure and tables for life and reliability testing (based on exponential distribution).
	NHB 5300.4	Safety, Reliability maintainability and quality provisions for the space shuttle program.
Medical	FAR 53.246-2	Federal acquisition regulation, inspection of supplies — fixed price.
	ANSI Z 1.15	Generic guidelines for quality systems.
	ANSI Z 1.8	Specification of general requirements for a quality program.
	ANSI Y 14.5	Dimensioning and tolerancing.
Nuclear	ANSI Z 1.8	Control chart method of controlling quality during production.
	GMP's	Good manufacturing practices regulations.
Software	NRC Title 10, CFR 50 & ANSI NQA-1	Nuclear quality assurance program requirements.
	ANSI 730	Software quality assurance plans.

At our manufacturing sites, local quality and manufacturing engineering organizations enforce these contractual programs and provide the cost and statistical process data to support our program of continuous quality improvement.

CQE supports Intel's systems sales and marketing engineers by reviewing customer requirements and negotiating the technical terms and conditions. Intel's field order entry systems, STARS (Sales Tracking and Reporting System), has special data fields to indicate if a customer's purchase order/contract has unique technical or quality requirements. This flag alerts our customer service representatives, who then contact the CQE contract review team for a response. Upon completion of the review, approvals from CQE are entered into STARS to implement the customer's order.

### Customer Audits

Intel complements its rigorous internal quality assurance audits with a philosophy of open-door customer audits. Customers are invited to visit corporate headquarters or site manufacturing facilities and to meet our quality and reliability organization. Customers may request presentations on our quality assurance program or receive tours of factory departments and product qualification laboratories. We invite customers to bring in specialists for in-depth evaluation of Intel inspection, raw materials control, workmanship standards and quality assurance policies and procedures.

### Certificates of Compliance (C/C's)

Because customers frequently require certificates of compliance (C/Cs), Intel Systems provides them with every product shipped (see Figure 6-20). The C/C is preprinted on Intel shipping papers and signed by an authorized quality assurance/plant clearance inspector.

<p style="text-align: center;"><b>CERTIFICATE OF COMPLIANCE</b></p> <p>The products shipped herewith have been inspected and comply with the requirement of your purchase order to the extent that such requirements have been accepted and acknowledged by Intel. Substantiating inspection and test data are on file.</p> <p style="text-align: center;">By _____ QA/Plant Clearance Inspector</p>
--

Figure 6-19. Certificate of Compliance

### CONCLUSION

Intel supports its customers with a World-Class Quality Assurance System. Our philosophy of Total Quality requires involvement by all employees to assure quality in our many processes, products and services. This employee involvement is a logically structured support activity that assures continuing satisfaction of customer requirements.



---

# Appendix

---





## APPENDIX

### STATISTICAL PROCESS CONTROL TOOLS

Statistical Process Control (SPC) tools are diverse, ranging from the simplest of problem-solving methods to the application of powerful statistical techniques. The use of any or all of these tools depends on the problem one is trying to solve. For example, there are process simplification tools that are used to reduce a complex process into manageable pieces. Once reduced, these pieces can be analyzed and controlled by the use of other tools. Once under control, different tools are used to provide breakthrough improvements in the process. Within Intel Systems Group, these tools are collectively thought of as the "SPC Toolkit," where each tool has its specific applications. See Figure A-1.

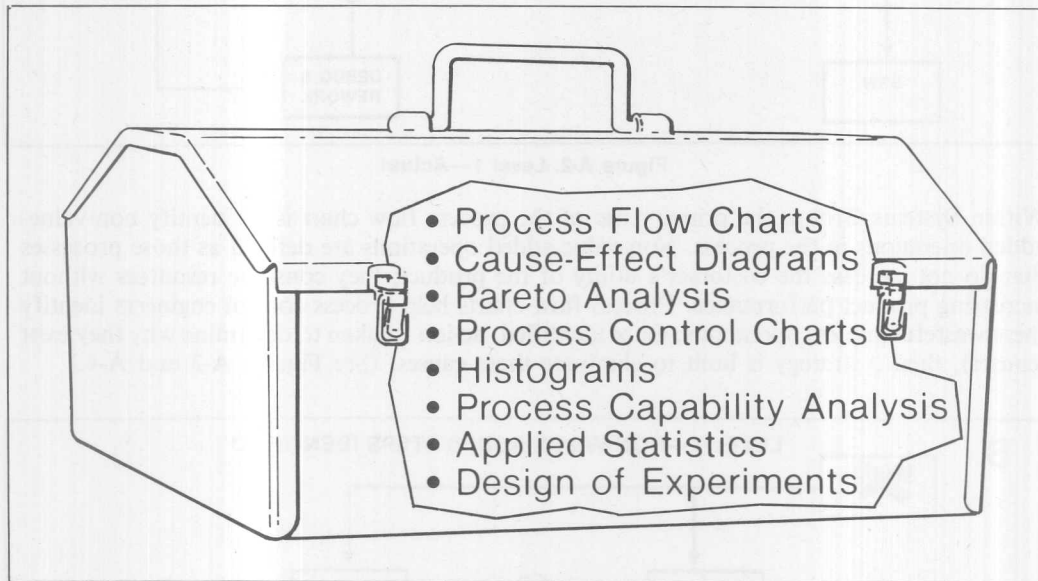


Figure A-1. Systems Group SPC "Toolkit"

All SPC tools share a common objective - the identification, characterization, control and reduction of *process variation*. By identifying and controlling process variation, the production process and the resulting product become predictable. This leads to the elimination of non-value-added operations such as inspection, test and audit. More important, however, is the realization of products that are both high in quality and cost-competitive.

#### PROCESS FLOW CHARTS

Process Flow Charts are used to break down complex processes into individual operations, functions, workstations and routines. This is a prerequisite to in-depth process analysis. There are two types of process flow charts: Level 1 and level 2 (see Figure A-2). Level 1 flow charts define a process as it presently exists (actual), while level 2 flow charts define a process as one would like it to be (goal). The differences between the two provides a "roadmap" for process improvements.

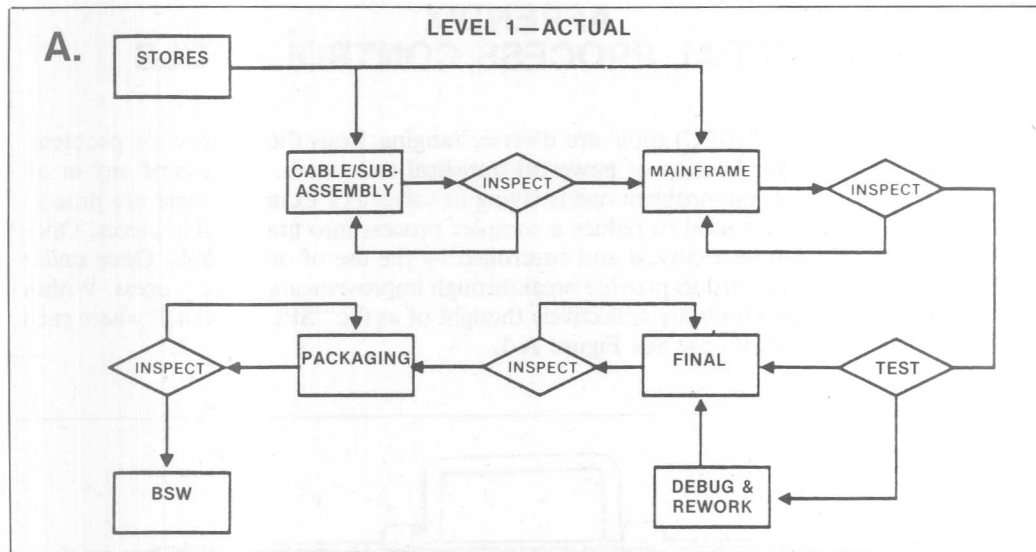


Figure A-2. Level 1—Actual

Within Systems Group, the primary use of the process flow chart is to identify non-value-added operations in the process. Non-value-added operations are defined as those processes that do not increase the customer's utility of the product; they consume resources without increasing product performance. Process flow charts help process control engineers identify these wasteful process operations. Once identified, action is taken to determine why they exist (causes), then a strategy is built to eliminate these causes. (See Figures A-3 and A-4.)

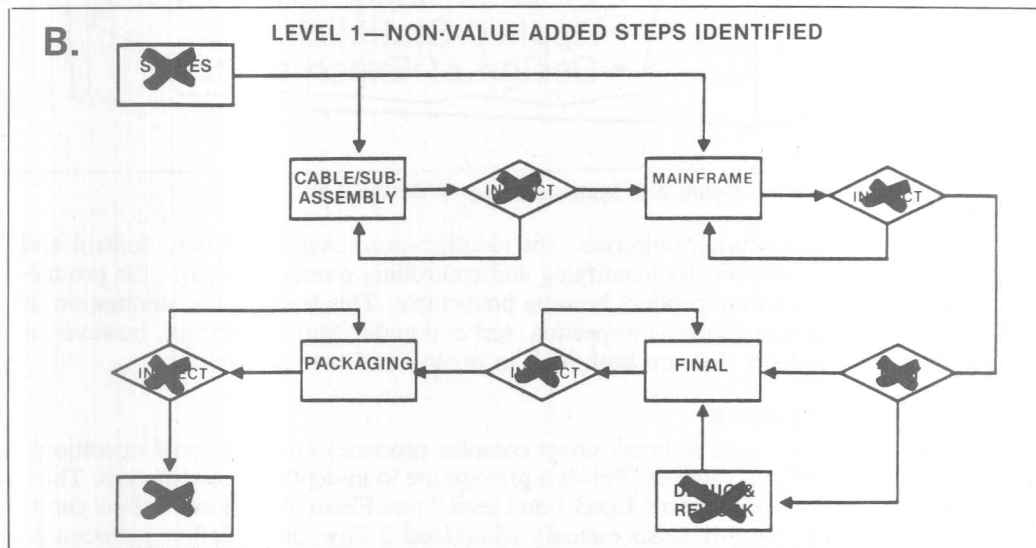


Figure A-3. Level 1—Non-Value Added Steps Identified

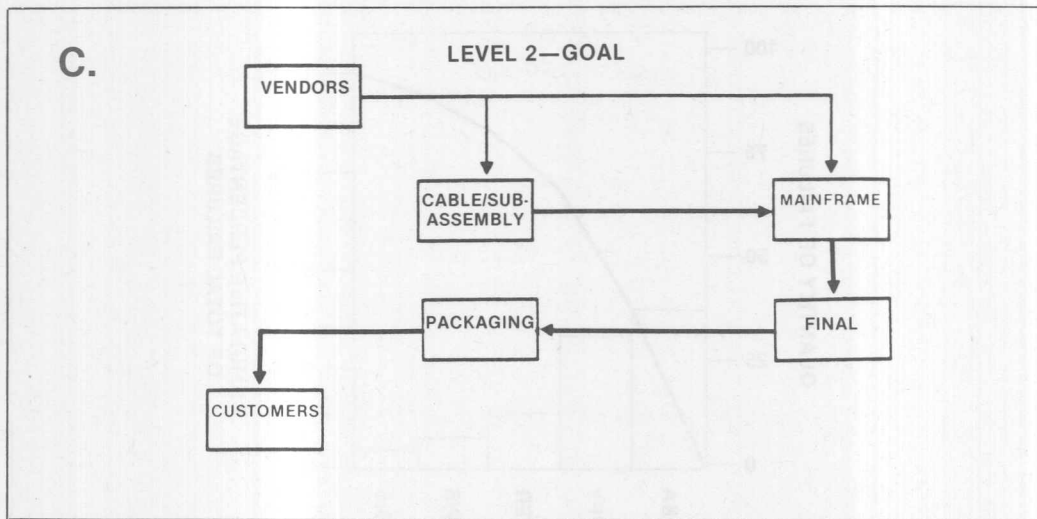


Figure A-4. Level 2—Goal

### PARETO ANALYSIS DIAGRAMS

Pareto analysis diagrams are used to identify the “vital few from the trivial many.” The theory behind their use involves the notion that in most processes there are always a few causes that result in most problems. This theory is also known as the 80-20 rule. Pareto analysis diagrams help management focus problem-solving efforts on the most important factors of economic process improvement. An example of an actual Pareto analysis diagram can be seen in Figure A-5.

### CAUSE-EFFECT DIAGRAMS

Cause-Effect diagrams have their origin in Japan where they have been used for quite some time. They are also known as fishbone (due to their resemblance to a fish skeleton) or Ishikawa (the originator) diagrams. Cause-Effect diagrams help:

- Identify individual causes of process (or product) variation
- Isolate the most important cause-effect relationships for further study
- Focus (limited) resources on the most important process parameters

When correctly used, Cause-Effect diagrams provide a fundamental understanding of what is happening in a process. They are an excellent tool for generating discussion between individuals or groups, such as Quality Control (QC) Circles. For example, Intel Systems Group typically initiates a new process improvement effort by establishing SPC teams. These teams begin by collectively generating a Cause-Effect diagram for the process in question. This procedure accelerates the identification of possible causes of process or product variation, while also providing a strong team-building atmosphere. An example of a team-generated Cause-Effect diagram is provided in Figure A-6.

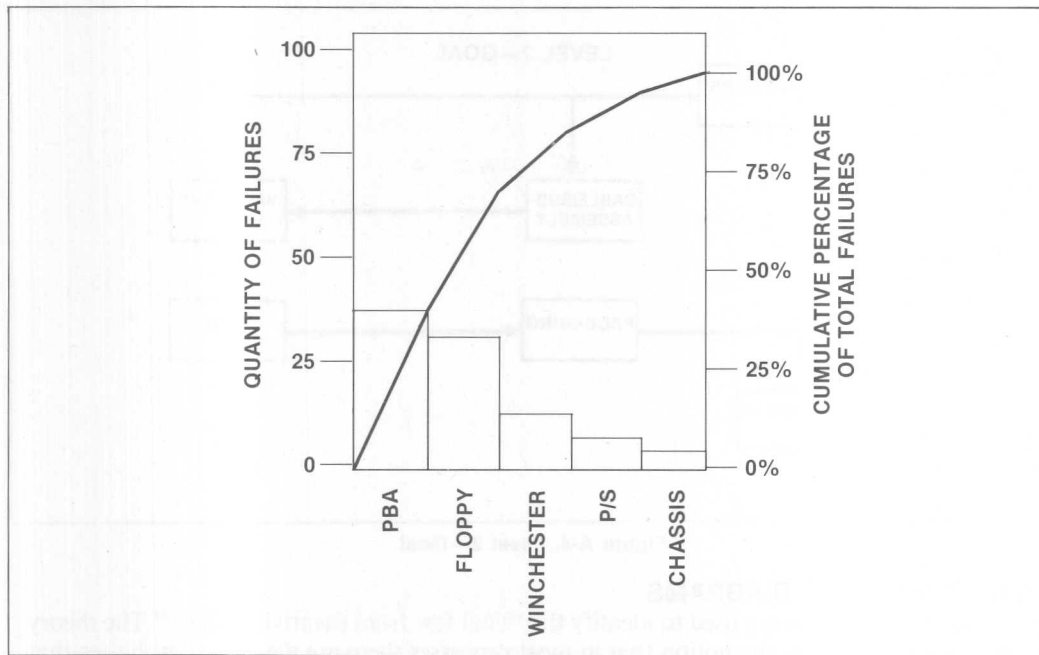


Figure A-5. Pareto Analysis Diagram of System Test Failures

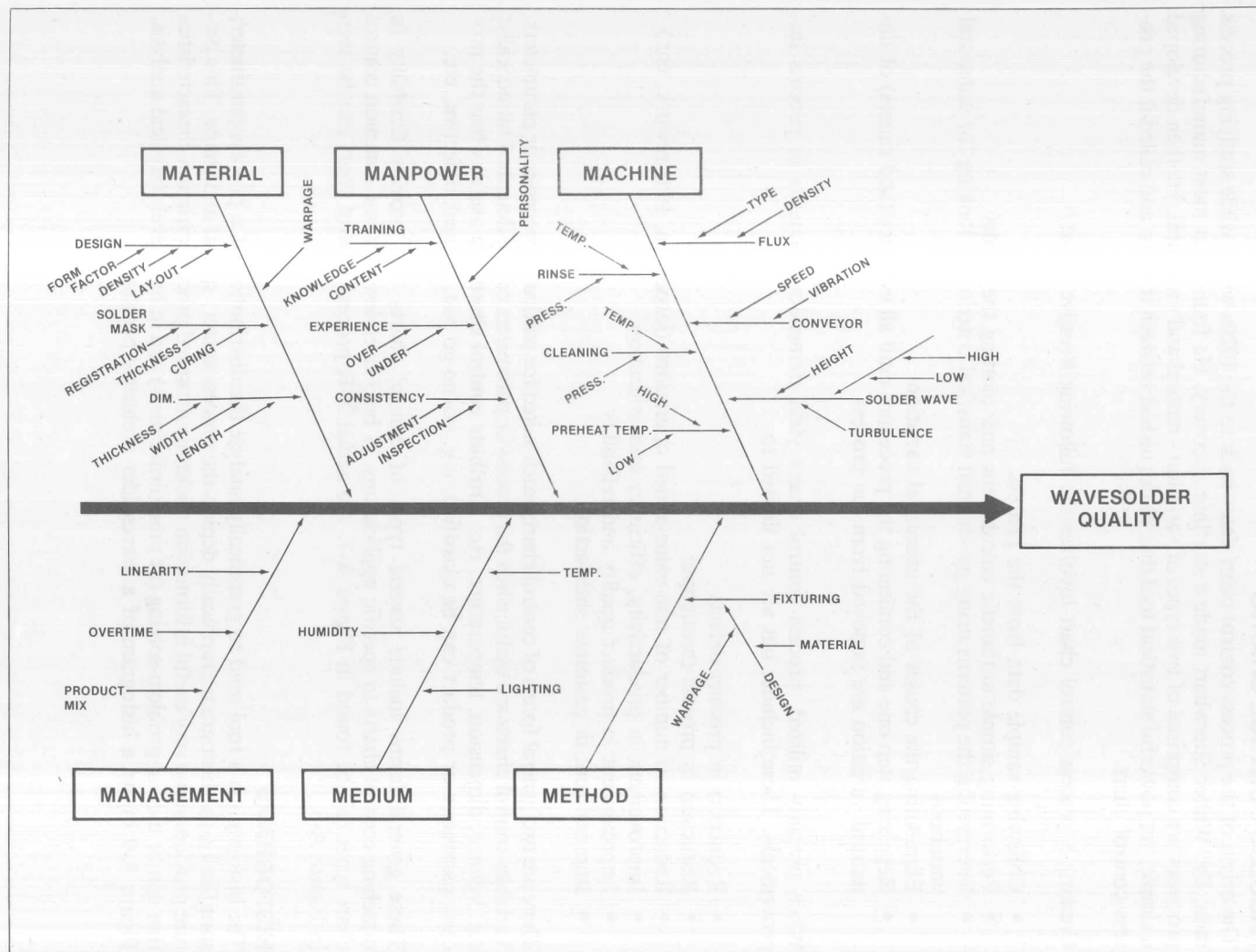


Figure A-6. Cause-Effect Diagram

## PROCESS CONTROL CHARTS

The origin of the process control chart dates back to the 1920s when, while studying process data, Dr. Walter Sherwhart made a startling discovery. He found that most manufacturing processes are comprised of two types of variation - natural and unnatural. He then developed a simple, yet powerful statistical tool that distinguished between the two and called it the process control chart.

Creating a process control chart involves the following iterative steps:

- Collecting sample data from the process
- Performing simple arithmetic calculations and plotting the results
- Interpreting the patterns using pre-defined statistical criteria and looking for unnatural variations
- Eliminating the causes of the unnatural variation
- Repeating step one and continuing the procedure until all evidence (and causes) of unnatural variation are removed from the process

When properly utilized, process control charts yield tremendous benefits in process improvements. These include, but are not limited to:

- Reduction in product defects
- Reduction in process throughput
- Reduction in number of non-value-added operations (inspection, test, rework, etc.)
- Improvement in productivity, efficiency and utilization
- Improvement in product quality and reliability
- Improvement in customer satisfaction

There are two general forms of control charts, each suited for particular processes or parameters. **Variables control charts** are useful when the process or parameters can be described numerically; e.g. voltage, dimension, temperature, etc. **Attribute control charts** are useful when the process, parameter or product can be classified; e.g. go/no-go test, percent defective, etc.

These general forms include several types of control charts that provide flexibility in matching control charts to specific applications. A brief overview of some common control chart types can be found in Figure A-7. An actual  $\bar{X}$ -R process control chart can be seen in Figure A-8.

## HISTOGRAMS

The histogram is a tool used to graphically analyze the distribution of a process parameter; specifically, the histogram graphically depicts the process center, spread and shape. This picture provides some very useful information about the nature of process variation characteristics that can be used in problem-solving (of unnatural causes) and in high-level statistical analysis. Figure A-9 shows a histogram of a wavesolder preheater parameter.

<b>Variables</b>	
• $\bar{X}$ -R Chart	Average and Range
• $\bar{X}$ - $\sigma$ Chart	Average and Standard Deviation (Sigma)
• Median Chart	Median and Range
• Individuals Chart	Actual Readings and Moving Range
<b>Attributes</b>	
• p Chart	Proportion Defective
• np Chart	Number of Units Defective
• c Chart	Number of Defects
• u Chart	Number of Defects per Unit

Figure A-7. Types of Process Control Charts

### PROCESS CAPABILITY ANALYSIS

Process capability is defined as the inherent natural behavior of a process after all sources of unnatural variation have been identified and eliminated. Thus, the capability of a process (or parameter) is the best it can perform over time when operating in a state of statistical control. Once identified, the process capability can be compared to the actual specifications.

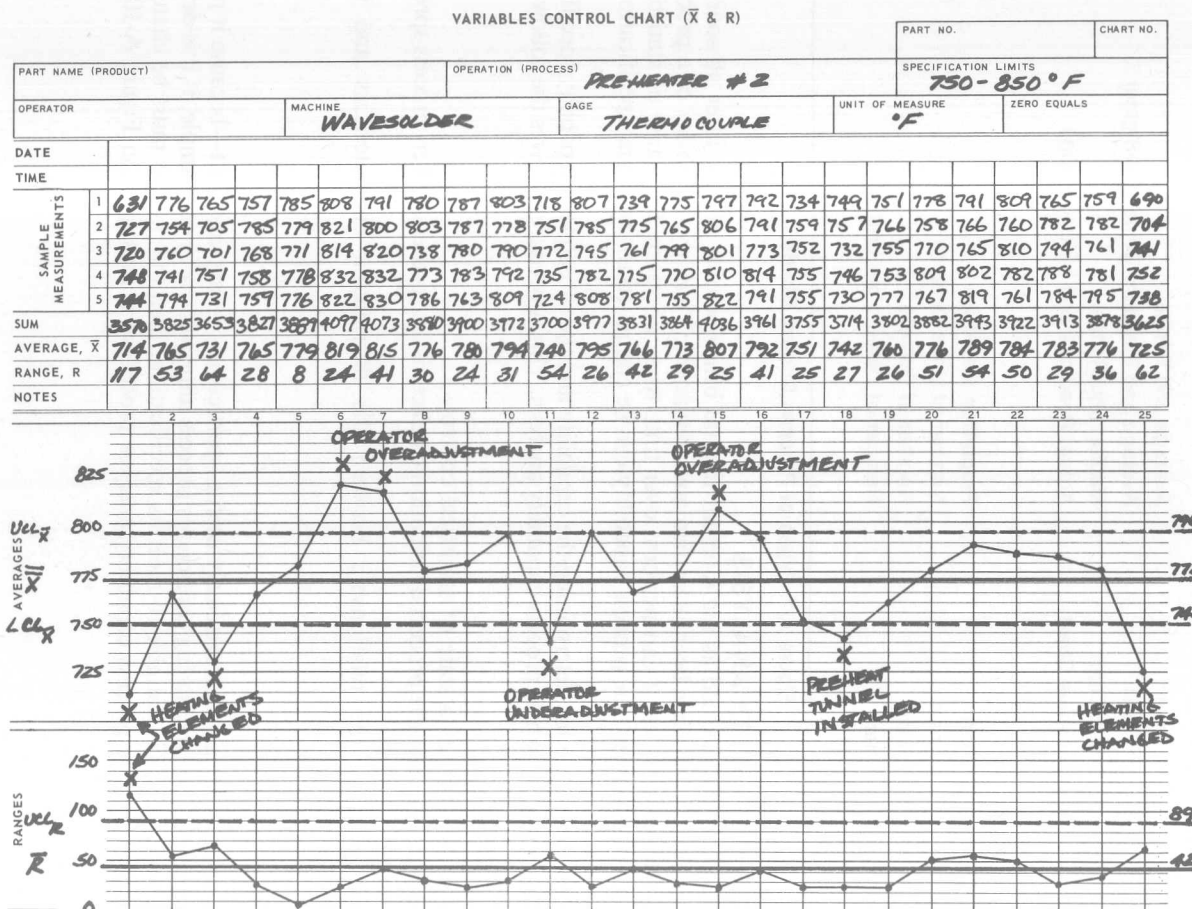
The general procedure for determining the capability and the subsequent capability specification evaluation is known as process capability analysis. This procedure involves the following three steps:

1. Demonstration of a state of statistical control.
2. Determination of the process distribution characteristics (process center, process spread & process shape).
3. Evaluation of the relationship between the distribution characteristics and the specifications.

Process capability analysis is extremely useful—particularly to management—because it provides the baseline for measuring continuous process improvement. For example, if it is determined that a process is not able to meet its specification, then the process must be changed by management. The process capability analysis procedure is illustrated in Figure A-10.



Figure A-8. Example of an  $\bar{X}$ R Control Chart



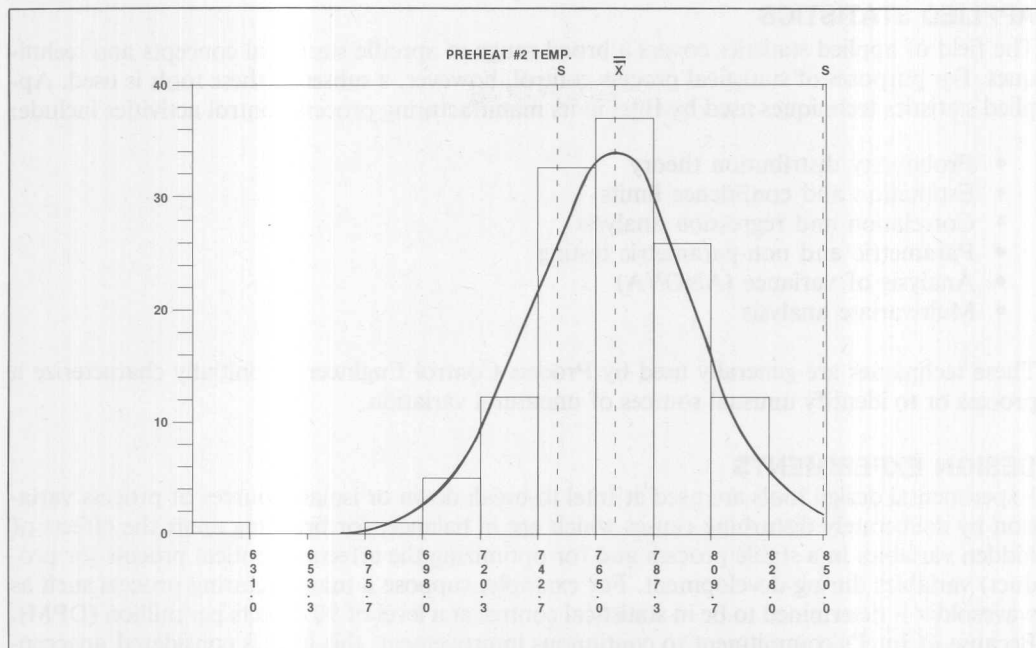


Figure A-9. Histogram Example

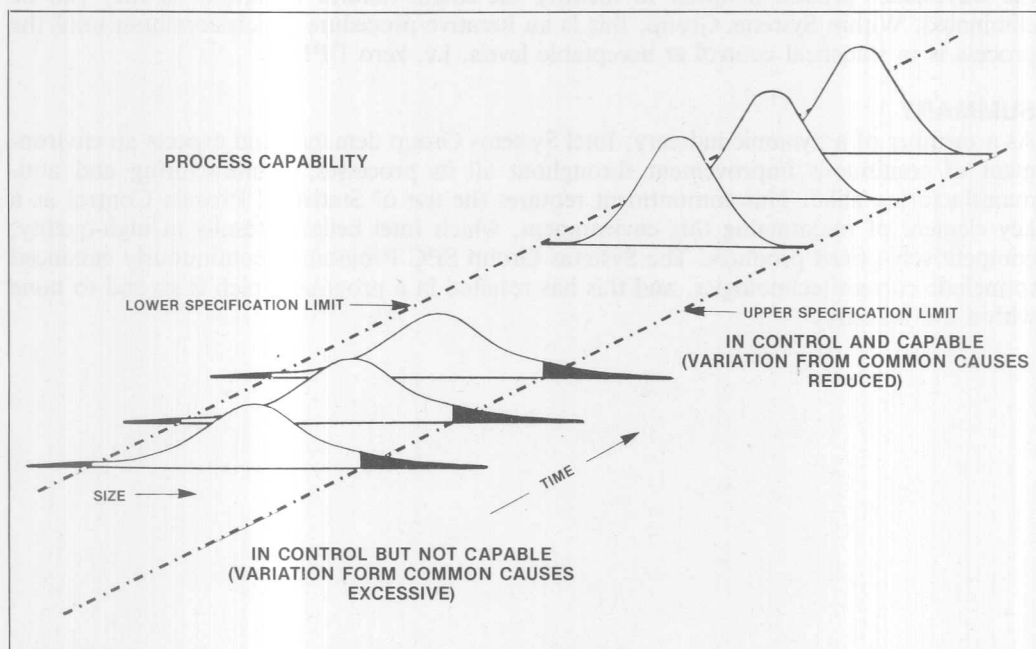


Figure A-10. Process Capability Analysis\*

\*from Ford Motor Co., "Continuing Process Control and Process Capability Improvement"

## APPLIED STATISTICS

The field of applied statistics covers a broad range of specific statistical concepts and techniques. For purposes of statistical process control, however, a subset of these tools is used. Applied statistics techniques used by Intel in its manufacturing process control activities include:

- Probability distribution theory
- Estimation and confidence limits
- Correlation and regression analysis
- Parametric and non-parametric testing
- Analysis of variance (ANOVA)
- Multivariate analysis

These techniques are generally used by Process Control Engineers to initially characterize a process or to identify unusual sources of unnatural variation.

## DESIGN EXPERIMENTS

Experimental design tools are used at Intel to break down or isolate sources of process variation by deliberately disturbing causes which are in balance, for breaking apart the effects of hidden variables in a stable process and for optimizing the effects of critical process (or product) variables during development. For example, suppose a manufacturing process such as wavesolder is determined to be in statistical control at a level of 90 defects per million (DPM). Because of Intel's commitment to continuous improvement, this level is considered unacceptable, despite the process being in control. A designed experiment is utilized to actually disturb the wavesolder process in order to identify the small, natural variations so they can be eliminated. Within Systems Group, this is an iterative procedure which continues until the process is in statistical control at acceptable levels, i.e. zero DPM.

## SUMMARY

As a member of a dynamic industry, Intel Systems Group demands and expects an environment of continuous improvement throughout all its processes, manufacturing and non-manufacturing alike. This commitment requires the use of Statistical Process Control as a key element of maintaining this environment, which Intel believes results in high-quality, competitively-priced products. The Systems Group SPC Program is continuously enhanced to include current technologies, and this has resulted in a program which is second to none within the industry.

---

# Glossary

---



## GLOSSARY

### A

**“A” Status:** Manufacturer’s item is acceptable for production procurement. There are no procurement limitations on quantity of these items.

**AE:** Activation energies (measured in electron volts).

**AGV:** Auto-guided vehicle.

**AML:** Approved Manufacturers List. Computerized listing of all approved manufacturers for each part used in Systems Group production.

**ANOVA:** Analysis of variance.

**ANSI:** American National Standards Institute.

**AQL:** Acceptable quality level.

**ATE:** Automated Test Equipment.

**ATP:** Acceptance Test Procedure.

**ASD:** Arizona Systems Division.

**ASRS:** Automated Storage and Retrieval System. Intel’s materials handling and control system.

### B

**Bellcore:** A reliability prediction procedure published by Bell Communications Research.

**BMS:** Bill of Materials System.

**BSW:** Board and Systems Warehouse (finished goods prior to shipment to customers).

**BTO:** Build To Order. Intel’s systems manufacturing configuration methodology, whereby products are assembled specifically per customer orders.

### C

**“C” Status:** Manufacturer’s item is acceptable for limited quantities with SQR’s approval.

**CAD:** Computer-aided design.

**CAM:** Computer-aided manufacturing.

**CBEMA:** Computer and Business Equipment Manufacturers Association.

**C/C:** Certificate of Compliance.

**CCE:** Corporate Components Engineering.

**CIM:** Computer-integrated manufacturing.

**Commodity Management:** Intel supplier methodology that integrates the purchasing, planning, manufacturing, engineering and quality groups to improve interaction with the supplier base.

**CPD:** Component part drawing.

**CQE:** Customer Quality Engineer.

**CSA:** Canadian Standards Association.

**CSO:** Customer Support Operation.

## D

**“D” Status:** Manufacturer’s item is not acceptable for any level usage.

**Derating:** Operating component parts at stress levels less than their maximum rated values to establish electrical and thermal operating parameters for the purpose of improving their reliability.

**DIP:** Dual In-Line Package.

**Dock-to-BSW:** Items from a manufacturer/supplier on this status can go directly to BSW after being received (needs SQE sign-off).

**Dock-to-Line:** Items from a manufacturer/supplier on this status can go directly to the Line after being received (needs SQE sign-off).

**DPM:** Defects per million.

**DPU:** Defects per unit.

**DTL:** Dock-to-Line. A logistics methodology whereby incoming materials move directly to the assembly line without incoming inspection. DTL status indicates a quality incoming product as well as on-time delivery.

**Dock-to-Stock:** Items from a manufacturer/supplier on this status can go directly to the line after being received (needs SQE sign-off).

**DTS:** Dock-to-Stock. A logistics methodology whereby incoming materials move directly to inventory without incoming inspection.

**Duty Cycle:** Ratio of active use time divided by total time.

## E

**“E” Status:** Manufacturer’s item is not acceptable for new design release. Items may be procured for pre-pilot or prototype or preproduction use. Design Engineering (DE) signature authorization is required on each engineering purchase requisition against “E” items. Items cannot be transferred to manufacturing stores until “C” or better status is achieved.

**ECL:** Emitter-coupled logic.

**EMI:** Electromagnetic interference.

**EPROM:** Erasable Programmable Read Only Memory.

**EPS:** External Product Specification. A document produced during any new product development cycle at Intel that specifies the product’s functional and physical attributes. Written while still in the planning phase.

**ESD:** Electrostatic discharge.

**ETL:** ETL Laboratories. A safety certification organization in United States.

## F

**Failure:** An equipment-caused inability to perform according to specification, requiring maintenance action or operator intervention to restore performance.

**Failure rate:** The number of failures per unit measure (time). The symbol used for failure rate is lambda ( $\lambda$ ).



**First point of sale:** The customer, dealer or distributor to whom product is first shipped.

**FCC:** Federal Communications Commission.

**FPA:** First-pass acceptance. A reliability rating assigned by Intel. For example, if 100 kits are tested and 96 finish without problems, the lot is said to have a 96% FPA.

**FQIT:** Field Quality Improvement Team. A field formed to coordinate and prioritize field quality problems between the production sites for corrective action.

**FSE:** Field Sales Engineer.

## G

**GPIB:** General Purpose Interface Bus.

**GPTF:** General Purpose Test Fixture, also known as a hot box.

## I

**IC:** Integrated circuit.

**iFICS:** Intel Factory Information Control System.

**iDIS:** Intel Database Information System.

**iMACS:** Intel Manufacturing and Materials Automated Control System. Intel's materials ordering and inventory control system, integrating inventory, billing of material, MRP and factory control data to provide comprehensive control of materials planning activities.

**I/O:** Input/Output.

**IQA:** Incoming Quality Assurance.

**iSBC:** Intel single-board computer.

**IMM:** Integrated Manufacturing Monitor, a test system comprised of Intel systems components used to design and implement custom tests for Intel custom-configured products.

**IR:** Infrared Oven.

**ITI:** Introduction to Intel.

## J

**JIT:** Just-in-Time.

## M

**MIL:** Military.

**MLRP:** Material Long Range Plan.

**MQE:** Materials Quality Engineering.

**MRP:** Materials Resource Planning.

**MTBF:** Mean time between failures. Unless otherwise stated, MTBF implies a constant failure rate. MTBF is found by summing total operating hours and dividing by the total number of chargeable failures.

**MTTF:** Mean time to failure. The average time until failure, measured from the first usage of the product until the occurrence of a failure. Used for parts considered non-repairable, such as integrated circuits.

## N

**“N” Status:** Items from this manufacturer/supplier shall not be purchased. This was an “A” (Approved Statused) manufacturer/supplier that was eliminated because of Vendor Base Reduction (needs SQE sign-off).

## O

**OEM:** Original equipment manufacturer.

**OHV:** Outside Hardware Vendor. A non-Intel facility manufacturing a board or systems-level product for Intel.

**OSD:** Oregon Systems Division

**OSV:** Outside Software Vendor. A non-Intel facility designing, coding, testing, debugging, documenting and manufacturing a software product for Intel.

## P

**PAL:** Programmable Array Logic.

**PCB:** Printed circuit board.

**PFEP:** Production Facility Evaluation Program. Intel factory audit program.

**PPSE:** Peripherals and Power Supply Engineering.

**PROM:** Programmable read-only memory.

**PSA:** Product Safety Auditor.

**PSC:** Intel Product Safety Council.

**PSE:** Product Safety Engineer; Power Supply Engineering

**PWB:** Printed wiring board.

## Q

**“Q” Status:** Has a 90-day maximum status, can only be put on by SQE. Requires a Quality Assurance Notice (QAN) that states all buying and usage requirements/restrictions.

**QA:** Quality Assurance.

**QAN:** Quality Assurance Notice. A document used to authorize and communicate quality actions such as product purges, holds, component alerts and special inspection instructions.

**Q/R:** Quality/Reliability.

**R**

**“R” Status:** Manufacturers listed are for reference only and are a guide for purchasing.

**Reliability:** The probability that a product will perform the intended functions within specified performance limits for a specified length of time while operating under specified environmental stress levels.

**RMA:** Return Material Authorization.

**S**

**“S” Status:** Can only be purchased by CSO to repair boards/systems (CCE or SQE sign-off).

**SBBL:** Static Burn-in at board level.

**SCT:** Systems Confidence Test.

**SDCC:** Systems Documentation Control Center.

**SDT:** Systems Diagnostic Test.

**Skip Lot:** An inspection rating indicating a quality level such that every other lot bypasses inspection and goes directly to inventory.

**SMT:** Surface-mount technology. Integrated circuit packaging technology that replaces through-hole-mounted components with surface-mounted components soldered by reflow and/or wave soldering processes.

**SQE:** Supplier Quality Engineering.

**SQR:** Systems Quality and Reliability.

**SPC:** Statistical Process Control. A statistical methodology for identifying, characterizing and reducing the amount of variation in a process.

**SPR:** Software Problem Report.

**SRE:** Systems Reliability Engineering.

**STARS:** Sales Tracking and Reporting System (commonly referred to as STAR).

**STBL:** System test at board level. Final board test for Intel products, performed in an edge-finger/backplane environment running at full product speed with voltage and temperature limits.

**STSL:** System test at system level.

**T**

**Traceability:** The ability to trace a finished product and/or its assembled parts from vendor point of origin to the first point of sale, and to trace a failed assembly in the field back to the original point of manufacture.

**THM:** Through-Hole Mount.

**TIPS:** Technical Information Phone Service.

**TTL:** Transistor-transistor logic.

**TUV:** Technischer Überwachungs-Verein. A product safety testing and certification organization for West Germany.

**U**

**UL:** Underwriters Laboratories, Inc.

**V**

**VDE:** Verband Deutscher Elektrotechniker. A German safety and EMI testing and certification organization.

**X**

**“X” Status:** Approved manufacturer that no longer manufactures the item (changed from \*).